HIGH DEFINITION X-RAY IMAGER TECHNOLOGY ROADMAP

Table of Contents

HDXI is one of three science instruments required for the *Lynx* mission, and will provide a wide field of view (0.15 degrees^2) with high angular resolution (~0.3-arcsecond pixels) optimally matched to the telescope point spread function. This document presents a roadmap for advancing the critical technology of the *Lynx* HDXI. The technology roadmap provides a description of the elements of the HDXI technology that need to be developed, identifies the maturation plan's key milestones, and the associated schedule, cost, and risk.

1 Introduction

This technology roadmap is a planning tool that lays out the steps, activities, and resources needed for maturing the High Definition X-ray Imager (HDXI) from the current State of the Art (SOA) through Technology Readiness Level (TRL) 5 by the end of project Phase A and to TRL 6 by Preliminary Design Review (PDR). The roadmap also serves to ensure that the instrument meets the scientific performance and programmatic requirements for the *Lynx* Observatory (Gaskin et al. 2019). This document contains the technology maturation schedule, cost, risks, and mitigation plans for technology maturation. The *Lynx HDXI Technology Roadmap* is considered a living document and will be updated as progress is made or conditions affecting the plan become known.

The *Lynx* HDXI design (Falcone et al. 2019) is derived from the highly successful Charge-Coupled Device- (CCD-) based X-ray imaging spectrometers built for the current generation of X-ray observatories, including the AXAF CCD Imaging Spectrometer (ACIS) instrument on the *Chandra* X-ray Observatory and the European Photon Imaging Cameras (EPIC) on the *X-ray Multi-Mirror* (*XMM*) mission. X-ray CCDs have been the workhorse of X-ray astronomy over the past two decades because of their high sensitivity over the soft X-ray band, their efficient rejection of charged-particle background, and their ability to create spectroscopically resolved images of the X-ray sky. The CCD sensor technologies used in ACIS and the EPIC cameras are inadequate to meet the scientific requirements of the *Lynx* mission for two reasons: the framerates are too slow, and the power requirements are too large. Substantial progress in Silicon (Si) sensor technology over the past 15 years has produced several promising options for HDXI, but none of these has yet been adapted to meet the instrument's demanding requirements for X-ray imaging spectroscopy. Thus, while it will fully exploit recent advances in sensor technology, HDXI requires significant additional technology development.

The *Lynx* science case is built upon three Science Pillars and the capability to return a wide range of additional observatory science (see *Lynx Concept Study Report*). The technical requirements of the HDXI are driven primarily by the first two of the Science Pillars while also being guided by the overall science case. These key scientific advances include revealing: (I) the Dawn of Black Holes and (II) the Invisible Drivers of Galaxy Formation and Structure. The relationship between these Science Pillars and technical instrument requirements is summarized in Table 1. For Science Pillar I, the HDXI will conduct a deep, wide-area survey. To do so efficiently, it must be able to detect point sources to a limiting flux of 10^{-19} ergs cm^{-2} s^{-1} in the 0.5 to 2.0 keV band over a ~480-arcmin^2 Field of View (FOV). The speed of this survey is directly proportional to the grasp (the product of the FOV and the effective area) required to reach this sensitivity in a given observation time. To achieve the required sensitivity and to identify detected sources unambiguously (i.e., without "source confusion"), the HDXI sensors must have a pixel size that oversamples the *Lynx* mirror's Point Spread Function (PSF) over this FOV. For Science Pillar II, the HDXI must be able to detect extended, low

surface brightness emission from haloes of nearby galaxies to a radius of >10 arcmin (roughly R_{500} for nearby galaxies) from the galaxy center. This second pillar places additional requirements on the HDXI, including background rejection efficiency, energy resolution (to separate emission from our galaxy from that of the target halo), and effective area in the energy band below 2 keV.

Table 1—HDXI requirements drivers from *Lynx* Science Pillars I and II.

Technology	Science Theme/Goal	Performance Driver	Instrument Requirements	
			Property	Value
HDXI	Pillar I: See the Dawn of Black Holes	Excellent spatial resolution over large FOV; Broadband X-ray quantum efficiency	Pixel size	0.33 arcsec
			Grasp at 1 keV	~600 m^2 $arcmin^2$
			Angular Resolution	<1 arcsec across FOV
	Pillar II: Reveal Invisible Drivers of Galaxy and Structure Formation	Large FOV; Good low-energy X-ray response; Low instrumental background	Effective area at 1 keV	2 m^2
			Energy resolution (FWHM) at 0.3 keV	70 eV
			Instrumental Background	<5 x 10^{-4} counts s^{-1} $arcmin^{-2}$ keV^{-1}
			FOV	22 x 22 arcmin

To achieve the *Lynx* science goals, two key elements of HDXI require additional technology development: (1) its X-ray photon-counting imaging sensors and (2) their associated readout electronics. Sensors convert incoming X-ray photons to electrical signals containing information about photon energy and interaction position. Readout electronics extract this information from sensor output signals and digitize it, and also provide the timing and bias voltages required by the sensor. Readout electronics are expected to be implemented with Application-Specific Integrated Circuits (ASICs).

This roadmap charts the development of three sensor technologies for HDXI. Hybrid CMOS sensors under development by Teledyne Imaging Systems use a thick, fully-depleted Si wafer bump-bonded to a Readout Integrated Circuit (ROIC) with multiple high-speed readouts, low power, and on-chip digitization (Hull et al. 2019). A monolithic CMOS sensor in development at Sarnoff Research Institute (Kenter et al. 2018) features in-pixel, high-responsivity sense nodes and on-chip digitization for fast, low-noise operation. An advanced, "digital" CCD being developed at MIT's Lincoln Laboratories combines CMOS-compatible operating voltages and high-speed, on-chip amplifiers with parallel CMOS signal chains for greatly increased framerate and lower power compared to *Chandra* CCDs (Bautz et al. 2019). Each of these sensor technologies is illustrated in Fig. 1.

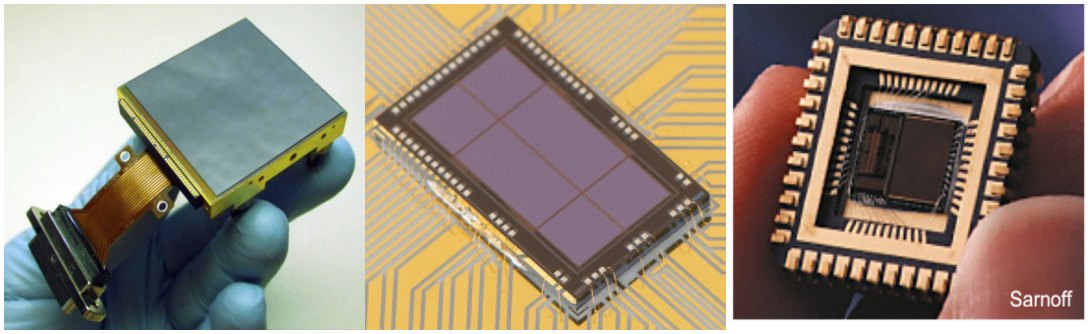


Fig. 1—Test devices representing the three sensor technologies under development for *Lynx* HDXI: (left) MIT Lincoln Lab's digital CCD, (center) the Teledyne/PSU hybrid CMOS sensor, and (right) the SRI/SAO monolithic CMOS sensor.

These technologies differ primarily in their architecture but not in their functionality; each has demonstrated proof-of-concept. At present, each of these technologies individually meets some, but does not simultaneously meet all, of the *Lynx* HDXI requirements, and each is assessed at TRL 3 for *Lynx* by the most recent Physics of the Cosmos (PCOS) Program Annual Technology Report. Each technology requires similar resources from the spacecraft, and all three have similar development paths. For purposes of development of the HDXI instrument concept for the *Lynx* Design Reference Mission (DRM), we have adopted one of these technologies: the hybrid CMOS sensor and associated ASIC. This choice was made because engineering interface information for existing components of this technology is publicly and readily available. As discussed below, the Advancement Degree of Difficulty (AD^2) of HDXI sensor technology is 5, so the development roadmap initially funds all three options to minimize risk (see §2.7). A downselection to two technologies will precede a final downselection prior to the start of Phase A.

Finally, while this technology roadmap was developed primarily for the HDXI, virtually everything contained herein applies to the *Lynx* XGS readout system as well, as is baselined for the DRM. Refer to §6 and §7 and the *XGS Technology Roadmap* for more detailed discussions of the XGS.

1.1 Lynx HDXI Overview

The *Lynx* HDXI architecture and technical requirements are derived from the *Lynx* Science Traceability Matrix (STM) which flows from the Science Pillars. A simplified block diagram of the instrument architecture in shown in Fig. 2. Key technical requirements are presented in Table 2.

The HDXI features a large focal plane of fast, low-noise, megapixel, X-ray photon counting silicon imaging sensors with 16-μm pixel pitch (0.3-arcsecond angular resolution) over a ~22-×-22-arcminute^2 FOV. It provides spectroscopic imaging with energy resolution of $E/\Delta E$~40 at 5.9 keV and ~4 at 0.3 keV. The DRM HDXI focal plane contains 21 sensors in a 5-×-5 arrangement with the corners vacant. The individual, flat sensors are tilted relative to one another to approximate the telescope's curved surface of best focus to maintain better than 1-arcsecond resolution (FWHM) over a ~480 arcmin^2 region of the FOV. The focal plane is passively cooled to ensure that there is no contribution to the noise from thermally generated electron-hole pairs. The temperature of the focal plane is approximately –90 °C and is stabilized to ±0.1 °C to ensure temporal stability of the system gain.

The sensors are driven by low-noise ASICs mounted on a Front-End Motherboard (FEMB). The ASICs provide the sensors with power and clocking, and perform signal processing functions. The ASICs must operate in close proximity to the sensors and are also passively cooled. Digital pixel data are transferred by the FEMB to the Detector Electronics Unit (DEU). Field Programmable Gate Arrays (FPGAs) within the DEU perform bias-level subtraction, event detection, and background discrimination. These science event data, plus engineering housekeeping data, are transferred to the DEU's processor board for packaging and transmission to the spacecraft data system. The DEU throughput is driven by the maximum count rate expected from the brightest diffuse X-ray sources in the sky (the Perseus cluster and the supernova remnant Cas A). Two primary modes of operation are anticipated: a full frame mode (the typical mode) in which each device is read at a rate of 100 frames per second, and a high-speed windowing mode in which a small region of one sensor is read with a frame-time of 100 μs to perform high-speed timing measurements of bright sources.

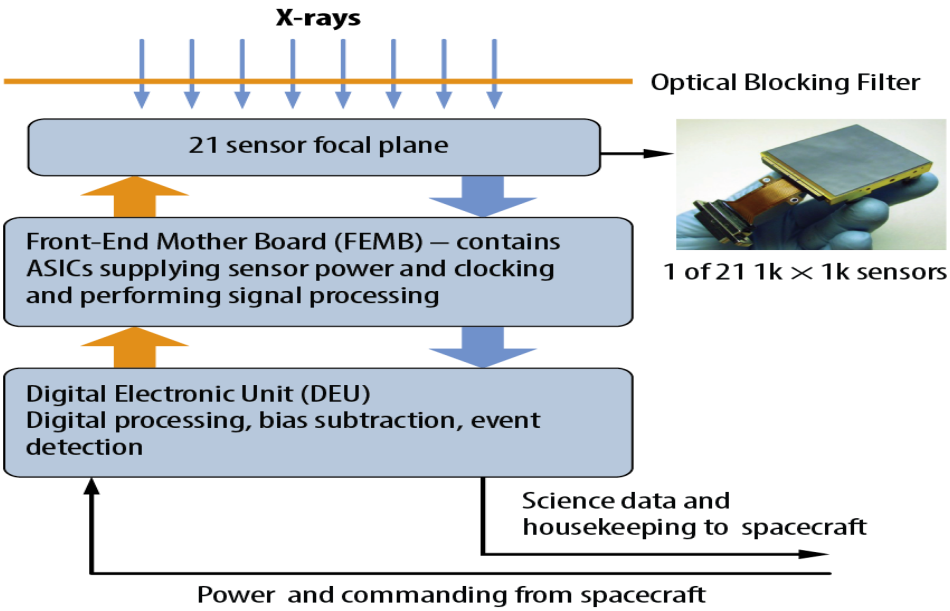


Fig. 2—Simplified HDXI block diagram.

Table 2—HDXI technical requirements.

HDXI Parameter	Requirement	Goal
Energy Range	0.2–10 keV	0.15–10 keV
Quantum Efficiency (excluding optical blocking filter)	≥0.85, 0.5–7 keV >0.1, 0.2–0.5 keV	≥0.9, 0.4–10 keV >0.2, 0.15–0.5 keV
Field of view	22 x 22 arcmin (5,000 x 5,000 pixels)	
Pixel size	16 x 16 μm (0.33 x 0.33 arcsec)	
Read noise	≤4 e^- (rms)	≤2 e^- (rms)
Energy Resolution	~70 eV (FWHM) at 277 eV	<40 eV (FWHM) at 277 eV
	<150 eV (FWHM) at 5.9 keV	<130 eV (FWHM) at 5.9 keV
Framerate—full frame	>100 frames s^{-1}	
Framerate—single 20-x-20-arcsec window	>10,000 windows s^{-1}	>100,000 windows s^{-1}
Radiation tolerance	10 years at L2	25 years at L2
Optical/UV Blocking	$>10^{-6}$ in U and V bands	
Full field event rate	>8,000 counts s^{-1}	>20,000 counts/s
Temporal resolution (20-x-20-arcsec window mode)	≤100 μs	≤10 μs

1.2 HDXI Detailed Description

The HDXI instrument design is described by Falcone et al. (2019). A detailed block diagram of the complete camera system as developed by NASA Marshall Space Flight Center (MSFC) Advanced Concepts Office (ACO) and further refined by the NASA Goddard Space Flight Center (GSFC) Instrument Design Laboratory (IDL)is shown in Fig. 3. The electrical architecture is shown in Fig. 4. The 21 sensors are housed in a vacuum enclosure so that they can be run on the ground at their nominal operating temperature of –90 °C. Heat pipes connected to a radiator provide cooling.

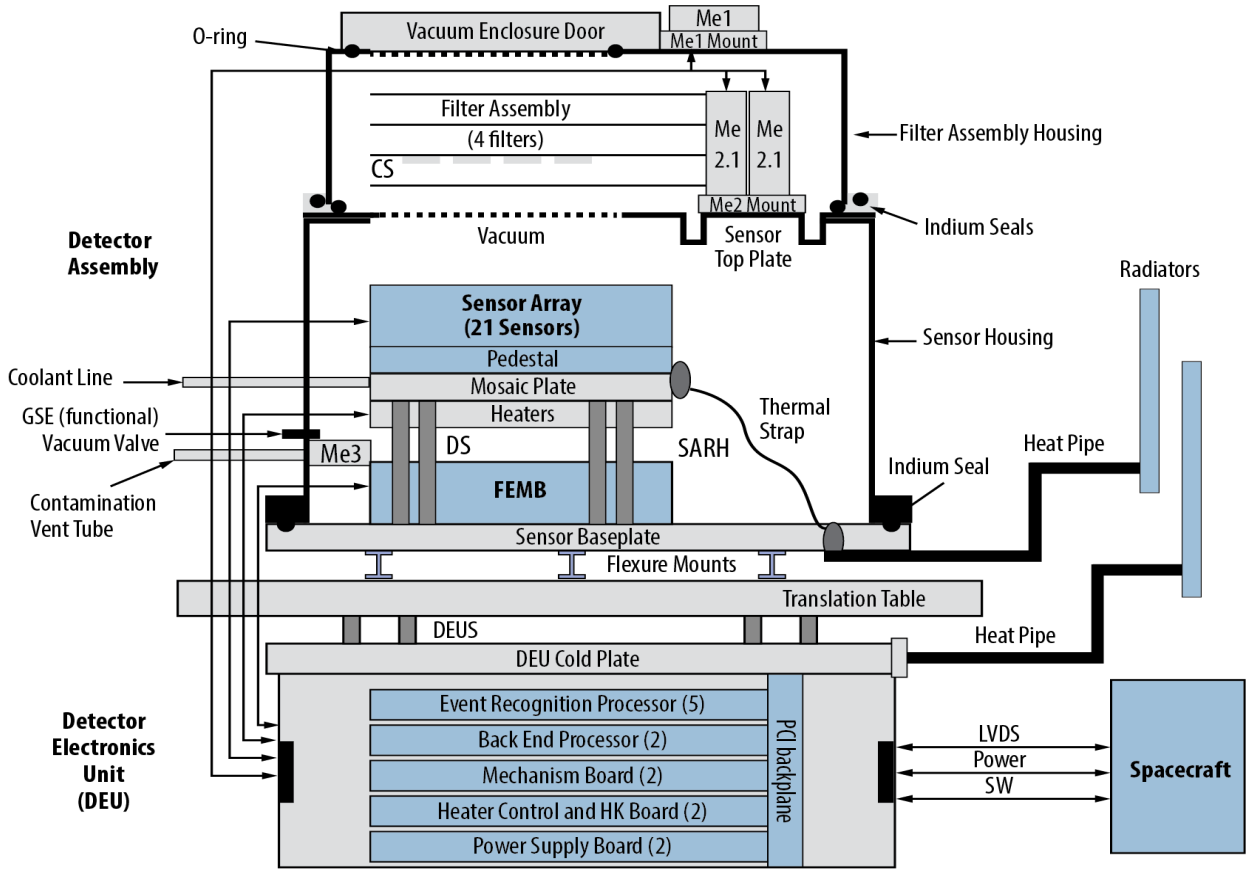


Fig. 3—Schematic diagram of the complete *Lynx* HDXI system developed by MSFC ACO and GSFC IDL. Refer to the *Lynx* DRM description for details.

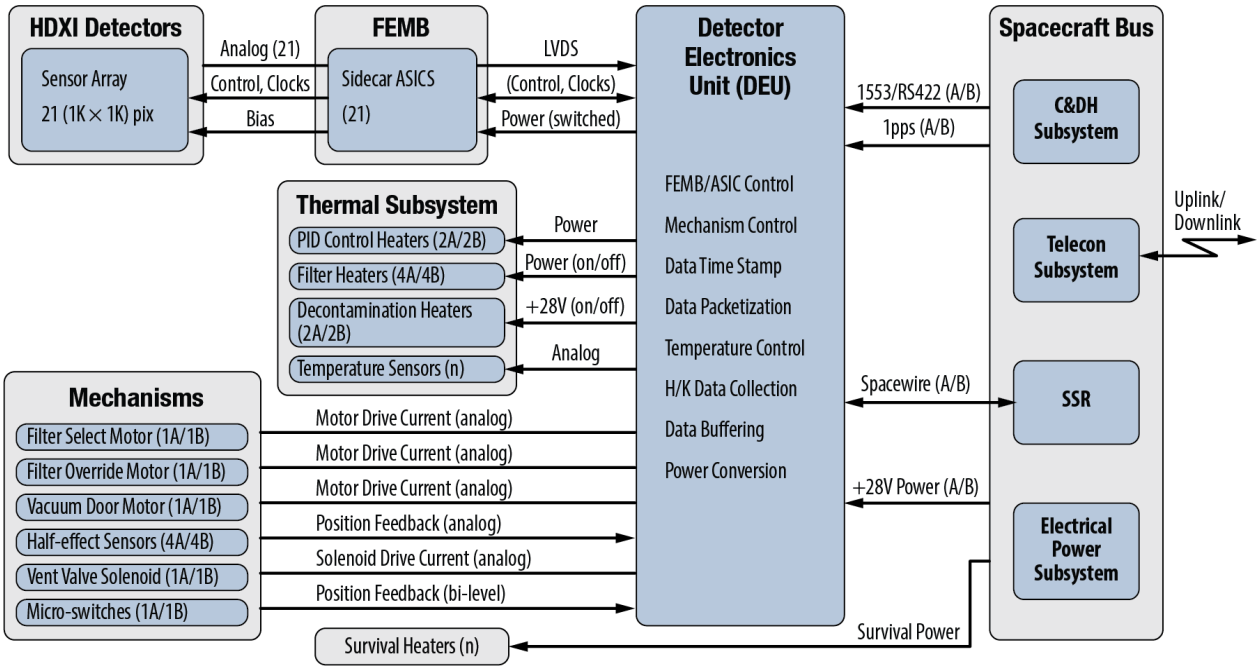


Fig. 4—*Lynx* HDXI architecture.

The vacuum housing also encloses a filter mechanism equipped with several filters for a range of optical blocking options as well as X-ray calibration sources. Effective contamination control is essential to maintaining the soft X-ray response required to meet *Lynx* science objectives, and a detailed contamination control plan has been developed. As part of the HDXI contamination control strategy, the filters are maintained at room temperature during operation to protect the cold sensor surfaces from molecular contamination. The filter mechanism includes a closed position that blocks all X-rays and soft protons from the telescope. A thin layer of Aluminum (Al) will likely be deposited on each sensor to provide a nominal level of optical blocking even in the filter open position.

The sensors are connected to an FEMB, which contains the ASICs that drive the sensors. The FEMB is located close to the focal plane (within the vacuum housing) to minimize noise on the analog lines and crosstalk between the digital signals. The FEMB in turn interfaces with the DEU, which configures the ASICs and receives the digital data. Event Recognition Processors (ERP) within the DEU extract events from the digital data stream. Each ERP consists of four FPGAs and associated electronics. The suite of ERPs has sufficient bandwidth to process the data from the twenty-one 1,000-×-1,000 sensors at a framerate of 100 Hz with substantial margin for redundancy. A multiplexing architecture allows digital data from any sensor to be processed by any ERP. The DEU receives commands from the spacecraft bus to configure and control the instrument and transmit housekeeping and science data. The DEU power supplies, bus controllers, and backplane are fully redundant.

The digital data from the detector assembly must be processed in real time so that only those pixels identified as candidate X-rays are sent to the spacecraft telemetry system to be transmitted to the ground. This results in 3 to 4 orders of magnitude reduction in the volume of data that must be telemetered. The instrument throughput and allocated telemetry bandwidth are sufficient to transmit data continuously from a source as bright as 8,000 counts/s. Both the detector assembly and the DEU are mounted to the *Lynx* Science Instrument Module's (SIM's) translation stage. The SIM provides focus capability.

Sensor "bias" (zero-signal) level computation and gain correction are done in the ERPs; the precise algorithms depend on the sensor technology but are derived from previous flight experience. Possible scenarios include creating a bias map before each observation (the technique used by the *Chandra* ACIS instrument) or maintaining a running average mean frame, or some combination of the two. The default mode of operation is to read out all sensors and apply an established event detection algorithm to bias-corrected frames to determine the position, pulse-height, and grade (i.e., morphology) of each X-ray event. Events that pass command-programmable filters in pulse-height and grade are transferred to the Observatory data system for telemetry to the ground. As noted above, the instrument also possesses a high-speed windowing mode in which a 20-×-20-arcsecond region of the FOV can be read out in <100 μs. This reduces photon pileup from very bright sources and allows high-resolution timing measurements of sources such as pulsars and magnetars. This windowing mode may be run simultaneously with the full frame mode so that events from the bright source are processed rapidly, but the entire FOV is also read out at the nominal ~100 frames s^{-1} cadence. Finally, the system can operate in a special mode to transfer full, unprocessed sensor frames to the ground for diagnostic purposes.

1.3 Technology State of the Art

HDXI requires further development in two technology areas: (1) silicon X-ray image sensors and (2) the ASICs that support them. The sensor converts each absorbed X-ray photon into a charge

packet that produces an analog electrical signal of amplitude proportional the X-ray photon energy. The ASIC "reads out" the sensor, processing raw sensor output signals to provide a low-noise estimate of the quantity of charge in each sensor pixel in each frame. It also provides various bias and timing signals required by the sensor.

The HDXI instrument was assessed to be TRL 3 by the NASA PCOS Technology Review Board in June 2016. Table 3 shows this rating along with a list of key advancements needed to reach TRL 6. The *Lynx* program agrees with this assessment. The TRL assessments apply to all three of the technical approaches (hybrid CMOS, monolithic CMOS, and digital CCD) under development for HDXI (see Fig. 1 and §1). Current sensor performance for each of these is compared with HDXI requirements in Table 4. The table shows that each of the candidate technologies has unique needs for further development. For the hybrid CMOS sensor, the key is to reduce readout noise and improve low-energy spectral resolution. For the monolithic CMOS sensor, the principal challenge is to increase the depletion depth to provide the required high-energy X-ray detection efficiency. For the digital CCD sensor, a significant increase in framerate is required.

Table 3—HDXI technology maturation elements.

Element #	Element Description	Current TRL	Key Advances Required
1	Silicon X-ray image sensors	3	• Reduce noise (Hybrid CMOS) • Increase depletion depth (Monolithic CMOS) • Increase framerate (Digital CCD)
2	Driver and signal processing application specific integrated circuits (ASICs)	3	• Optimize readout/control functions (sensor-specific) • Optimize operating temperature • Develop flight packaging

Table 4—HDXI sensor requirements and current performance.

Parameter	Requirement	Current Performance		
		Hybrid CMOS	Monolithic CMOS	CCD
Pixel size (μm)	≤16	12.5	16	8
Spectral resolution (eV, FWHM) at 0.5 keV at 6 keV	 70 150	 78 (at 0.5 keV) 156 (at 5.9 keV)	 60 eV (at B Kα 183 eV) 150	 N/A 145
Read noise (electrons, RMS)	≤4	5.6	2.9	4.2
Single sensor framerate (frame s^{-1}) x (frame size Mpixel)	≥100 x 1	>100 Mpix/s (small prototype) (full size >100 x 1 Mpix breadboard in design)	20 frames s^{-1} x 1 Mpixel	4.7 x 0.5
Depletion Depth (μm)	≥100	100	15	75
ASIC status		Representative ASIC developed; improvements planned	In development	Breadboard in design

N/A: measurement not available

While the PCOS board did not assess AD^2, the *Lynx* program performed an internal non-advocate assessment that placed the overall AD^2 at 5 based on the SOA of the sensor technologies. While there are no known physical barriers to carrying any of the candidate technologies to TRL 6, engineering judgment and lessons learned from past programs like *Chandra* form the basis for carrying three options into the program with successive downselections to a single technology path in Phase A.

ASIC requirements and sensor/ASIC interfaces are sensor-specific. The technical approach for each, however, is relatively straightforward, and the internal review noted above assessed the AD^2 at 2. However, experience of other similar programs (e.g., *WFIRST* and *Athena*) shows that ASIC development must be closely coupled to sensor development and so parallel development efforts will continue until downselections are made.

2 Detailed Technology Roadmap

Table 5 provides the detailed TRL advancement roadmap planned for the *Lynx* instrument along with AD^2 descriptions. The left hand column provides an overall description of the development effort. The three columns to the right provide milestone designators, descriptions, and target dates. The highlighted milestones denote major program progress achievements and were used as the basis of the program schedule chart (see Fig. 5).

2.1 Key Milestones

Table 5—HDXI TRL Milestones.

TRL 3 -> 4, Advancement Degree of Difficulty (AD^2): 5 – As discussed in §1.3 above, significant sensor development efforts will be required to meet *Lynx* goals. Three sensor technology candidates (along with associated ASIC technology) have been identified. While all are projected to be capable of meeting Lynx requirements, all three are in funded development cycles at this point. This is in accordance with the NASA AD2 definition and formal decision-making processes will be employed to down-select at specific program junctures in testing. The final downselection will be made at/near the beginning of Phase A.
Anticipated date to achieve TRL 4: 10/1/2024

NASA TRL 4	**System/component breadboard built and operated to demonstrate basic functionality and critical test environments. Associated performance predictions are defined relative to the final operating environment.** **Breadboard: A unit that demonstrates function only, without respect to form or fit in the case of hardware, or platform in the case of software. It often uses commercial and/or ad hoc components. Operated to provide basic proof of concept but not intended to provide definitive information regarding operational performance.**

Lynx HDXI TRL 4 Exit Criteria

A low fidelity breadboard sensor must demonstrate a credible technology development path to the required on-orbit performance of the *Lynx* HDXI. Demonstrations must trace to the on-orbit performance requirement in the operational environment. System/component performance is consistent with the expected flight performance, given no worse than a 50% uncertainty in lab demonstrations and models (as prescribed by PCOS), consistent with the low-fidelity system required for TRL 4.

A credible demonstration must include the following:

1. A credible sensor performance budget.
2. Laboratory demonstration of breadboard sensor array with the following characteristics and performance:
   - Pixel size no larger than flight requirement.
   - Back-illuminated-equivalent with X-ray quantum efficiency and resolution.
3. Laboratory demonstration of a breadboard signal processing ASIC with the following characteristics:
   - Electrically compatible with the brassboard sensor array
   - Meets system (sensor array + ASIC) noise requirements when operated within a factor of 2 of required readout rates over a single channel

HDXI/Development Maturation Milestones

#	Milestone Description	Date
Pre-TRL4-1	1st evaluation complete on 1st set of sensor/ASIC pairs from vendors	NLT 7/1/22
Pre-TRL4-2	1st evaluation complete on 2nd generation of sensor/ASIC pairs from vendors	NLT 4/1/23
S1	Demonstrate required single-channel sensor noise performance at required pixel rate	NLT 4/1/2024
S2	Demonstrate required single channel sensor spectral resolution and quantum efficiency at 5.9 keV (energy of standard Fe^{55} source)	NLT 4/1/2024
S3	Demonstrate single-channel sensor spectral resolution and quantum efficiency at 0.3 keV (at energy of C Kα line)	NLT 4/1/2024

Under the following conditions: • in vacuum over a range of realistic detector operating temperatures (e.g. –30 < T < -100 C) • non-flight interconnects between ASIC and sensor array	S4	Confirm required sensor noise, resolution, and quantum efficiency meet requirements at high and low energies in single-channel sensor, and validate sensor performance model	NLT 6/1/2024
4. Model predictions • optimum detector operating temperature given radiation tolerance results	Pre-TRL4-3	Downselection from 3 to 2 technologies following SME review	NLT 7/1/23
• optimum allocation of noise and responsivity/gain between sensor array and ASIC	Pre-TRL4-4	First evaluation complete for 3rd generation sensor/ ASIC pairs from vendor	NLT 4/1/24
• optimum trade-off between depletion depth and low-energy spectral resolution as a function of detector noise and pixel size	S5	Demonstrate required sensor noise, resolution, and quantum efficiency at high and low energies in representative multi-channel sensor	NLT 10/1/2024
	S6	Assure required performance of a representative multi-channel sensor after exposure to flight ionizing and non-ionizing radiation environment, using test and/or analysis	NLT 10/1/2024
	A1	Demonstrate required single-channel ASIC noise performance	1/1/2023
	A2	Demonstrate required ASIC noise level in multi-channel ASIC of representative scale	6/1/2024
	A3	Assure required ASIC radiation tolerance, using test and/or analysis	10/1/2024
	Pre-TRL4-5	Downselection to single technology following SME review	NLT 10/1/24

TRL 4=>5, Advancement Degree of Difficulty (AD^2): 3

At this point, the fundamental capability of the selected technology has been demonstrated (exit criteria for TRL 3 to TRL 4 transition) and development efforts will focus on the assembly and testing of larger sensor/ASIC arrays with higher fidelity testing with respect to flight conditions. The engineering development in this stage will be more straightforward than in the TRL 3 to TRL 4 stage with fewer unknowns and lower risk. Increasing array size once the fundamental technology characteristics have been demonstrated has been demonstrated in many analogous scientific and commercial development and so is not expected to pose major risks to the program.

Anticipated date to achieve TRL 5: July 1, 2026

NASA TRL 5	**A medium fidelity system/component brassboard is built and operated to demonstrate overall performance in a simulated operational environment with realistic support elements that demonstrate overall performance in critical areas. Performance predictions are made for subsequent development phases.** **Brassboard: A medium fidelity functional unit that typically tries to make use of as much operational hardware/software as possible and begins to address scaling issues associated with the operational system. It does not have the engineering pedigree in all aspects but is structured to operate in simulated operational environments in order to assess performance of critical functions**

Lynx HDXI TRL 5 Exit Criteria

Must demonstrate a credible technology development path to the required on-orbit performance of the *Lynx* HDXI. Demonstrations must trace to the on-orbit performance requirement in the operational environment. System performance is consistent with the expected flight performance, given no worse than a 30% uncertainty in lab demonstrations and models (as prescribed by PCOS), consistent with the medium-fidelity system required for TRL 5.

A credible demonstration must include the following:

1. Laboratory demonstration of a brassboard sensor array with the following characteristics and performance:
   - Pixel size no larger than flight requirement.
   - format and area at least one-quarter of required full-scale
   - representative number of parallel outputs, with a clear path to scaling to meet flight framerate requirement
   - operating with required readout rate with required noise with brassboard ASIC (see below)
   - back-illuminated with X-ray quantum efficiency and resolution meeting of flight requirements.

   Under the following conditions:
   - In vacuum at optimum (predicted) detector operating temperature
   - Un-irradiated and after required radiation dose
2. Laboratory Demonstration of a sensor-array compatible multi-channel brassboard signal-processing ASIC with the following characteristics and performance:
   - Channel multiplicity matching brassboard sensor array
   - System (sensor + ASIC) noise performance meeting required noise level at required readout rate.

   Under the following conditions:
   - Representative electrical connections between sensor array and ASIC
   - Representative sensor array and ASIC temperatures
   - At least two sensor/ASIC pairs operating in close proximity representative of a flight focal plane.
3. Model calculations/ predictions:
   - Validate optimum detector operating temperature prediction
   - Validate spectral resolution and quantum efficiency at flight depletion depth
   - Predict flight focal plane and ASIC power dissipation and cooling requirements

HDXI/Development Maturation Milestones

#	Milestone Description	Date
SA1	Delivery of brassboard sensor/ASIC combination from vendor to begin TRL 5 testing	NLT 10/1/25
SA2	Demonstrate required performance of integrated sensor/ASIC system or representative size	10/1/2025
SA3	Execute vibration, acoustic, and thermal cycling tests and demonstrate that subsequent performance continues to meet requirements of SA1 and those of S1–6 and A1–3	7/1/2026
SA4	Demonstrate that the above requirements continue to be achieved following required radiation dose	7/1/2026
SA5	Complete TRL 5 certification after SME review	7/1/2026

TRL 5=>6, Advancement Degree of Difficulty (AD^2):
At this point, the selected sensor/ASIC technology has met performance requirements in all key areas (e.g., energy resolution, noise, cross talk, etc.) using near-protype units with multiple sensor pairs. Straightforward engineering processes demonstrated on multiple successful programs will be tailored for the development of the EM unit for testing across the full range of anticipated space-like conditions in a configuration representative of the HDXI focal plane.

Anticipated date to achieve TRL 6: 1 November 2027

NASA TRL 6	**A high fidelity system/component prototype that adequately addresses all critical scaling issues is built and operated in a relevant environment to demonstrate operations under critical environmental conditions.** **Prototype: Unit demonstrates form, fit, and function at a scale deemed representative of the final product operating in its operational environment. A subscale test article provides fidelity sufficient to permit validation of analytical models capable of predicting the behavior of full-scale systems in an operational environment.**

Lynx HDXI TRL 6 Exit Criteria

The system must be demonstrated using a high-fidelity, scalable, flight-like prototype which adequately addresses all critical scaling issues and ensures all *Lynx* performance requirements are met in critical environments.

A credible demonstration must comprise the following:
1. Prototype Characteristics:
   - An array of flight-sized sensors and ASICs providing at least 1/4 of total focal plane area mounted in a realistic geometry
   - Flight-like sensor and ASIC packages and flight-like sensor-to-ASIC electrical interconnects
2. Environmental Testing
   - Acoustic (blocking filter only), thermal vacuum, vibration, radiation, and X-ray testing, as appropriate, in operational environments

HDXI/Development Maturation Milestones

#	Milestone Description	Date
SA6	Delivery of Engineering Model sensor/ASIC unit with multiple co-mounted sensor/ASIC arrays from vendors for evaluation following SME review	7/1/27
SA7	Demonstrate required performance of 5 sensor/ASIC systems in relevant environment	7/1/2027
SA8	Execute vibration, acoustic, and thermal cycling tests and demonstrate that subsequent performance continues to meet requirements of SA1 and those of S1–6 and A1–3	11/1/2027
SA9	Demonstrate that the above requirements continue to be achieved following a 10-year equivalent radiation dose	11/1/2027
SA10	Certify Engineering Model at TRL 6 at PDR (exit Phase B)	11/1/27

2.2 Milestones for TRL 4

Milestone Pre-TRL 4 1 — First evaluation complete on first set of sensor/ASIC pairs (all three technologies) from vendors.

Significance — First-generation test articles (science grade—electronically verified) from vendor available for HDXI-specific testing, and initial science laboratory evaluation supports next-generation design.

Verification — Laboratory measurement of key performance parameters (e.g., quantum efficiency, readout rates, noise levels, etc.) to characterize the sensor/ASIC pairs to the level needed to guide next-generation development. Test results compared to analytical model to drive next-generation model enhancement.

Milestone Pre-TRL 4 2 — First evaluation complete on second set of sensor/ASIC pairs (all three technologies) from vendors.

Significance — Second-generation test articles (science grade—electronically verified) from vendor available for testing to guide downselection to two technologies.

Verification — Laboratory testing for key performance parameters (as in Milestone 2.2.1) with sufficient fidelity to project operational performance of each sensor/ASIC pair as inputs to downselection process.

Milestone S1 — Demonstrate single-channel sensor noise performance at required single-channel pixel rate.

Significance — Establish that on-chip sense-node circuit design and performance are consistent with sensor performance requirements.

Verification — Analytical assessment of component (sensor, ASIC, and other system elements) level noise characteristics and development plan with quantified noise level targets to meet system requirements with margin. Laboratory measurement of a single sensor output channel read noise at required read rate. Demonstration of successful operation over the range of temperatures anticipated in flight.

Milestone S2 — Demonstrate required single-channel sensor spectral resolution and quantum efficiency at 5.9 keV.

Significance — Establish sensor depletion depth and bulk charge collection efficiency sufficient to meet required performance at energies above ~2 keV with margin.

Verification — Laboratory measurement of X-ray quantum efficiency and spectral resolution at 5.9 keV (e.g., using standard Fe^{55} source) of a sensor of representative array size (format), flight pixel size, and depletion depth to demonstrate that X-ray detection efficiency and spectral resolution requirements are met. Measurements must be made with noise and readout rates per Milestone S1 and must include accurate characterization of split-event fractions. Measurements must be made over representative detector operating temperature range per Milestone S1. Analytical assessment (sensor model backed by experimental testing) projecting acceptable full-size array performance (including anticipated event branching ratios).

Milestone S3 — Demonstrate single-channel sensor spectral resolution and quantum efficiency at 0.3 keV.

Significance — Establish that sensor "entrance window" passivation and associated fields are adequate to ensure required performance at energies below ~2 keV.

Verification — Laboratory measurement of X-ray quantum efficiency and spectral resolution at 0.3 keV of a sensor of representative array size (format), flight pixel size, and depletion depth entrance window passivation, with representative directly deposited Optical Blocking Filter (OBF), to demonstrate that X-ray efficiency and spectral resolution requirements are met. Measurements must be made with noise and readout rates per Milestone S1 and must include accurate characterization of split event fractions. Measurements must be made over representative detector operating temperature range per Milestone S1. Validation of sensor performance model (experimental and model result convergence) at sufficient fidelity to provide high-confidence projection of performance to other energies and to full-size array (including event branching ratios).

Milestone S4 — Confirm required sensor noise, resolution, and quantum efficiency at high and low energies in single-channel sensor, and validate sensor performance model.

Significance — Establish that sensor output amplifier, internal fields and entrance window support flight requirements, and that sensor performance model is validated over a range of energies.

Verification — Laboratory measurement of a sensor of representative array size (format), flight pixel size, depletion depth, entrance window passivation, with representative directly deposited OBF, to demonstrate that X-ray efficiency and spectral resolution requirements are met. Measurements must be made with noise and readout rates per Milestone S1 and must include accurate characterization of split event fractions. Measurements must be made over representative detector operating temperature range per Milestone S1. Validation of sensor performance model (experimental and model result convergence) at sufficient fidelity to provide high-confidence projection of performance, including charge sharing to other energies and to full-size array.

Milestone Pre-TRL4 3 — First downselection process (three technology candidates to two) complete.

Significance — At this milestone, a formal downselection from 3 to 2 sensor/ASIC technologies is complete.

Verification — Formal decision-making process (e.g., Kepner-Tregoe or Analytic Hierarchy) application with participation of non-advocate Subject Matter Experts (SMEs).

Milestone Pre-TRL4 3 — First evaluation complete for third-generation prototype sensor/ASIC pairs from vendors.

Significance — Program possession third-generation prototype, electrically verified units from vendor to be subjected to focused testing in support of a final downselection decision.

Verification — Sufficient laboratory testing for key performance parameters (sensitivity, readout rates, noise levels, etc.) to characterize the prototype units to a level sufficient to project operational characteristics and identify remaining development issues. Test results/analytical model comparisons to demonstrate consistency.

Milestone S5 — Demonstrate required sensor noise, resolution, and quantum efficiency at high and low energies in representative multichannel sensor.

Significance — Establish that required sensor performance is achieved with multiple output channels operating in parallel.

Verification — Laboratory measurement at multiple X-ray energies spanning the required HDXI pass passband. Sensor must be of representative array size (format), flight pixel size, and depletion depth entrance window passivation, with representative directly deposited OBF, with representative number of output channels (sensor dependent) reflecting engineering assessment of plausible performance impacts (e.g., crosstalk, excess noise) of multichannel operation. Measurements must be made with noise and readout rates per Milestone S1 and must include accurate characterization of split event fractions. Measurements must be made over representative detector operating temperature range per Milestone S1. Updated sensor performance model including impact of multichannel operation validated at earlier milestones to allow high-confidence projection of performance to other energies and to full-size array.

Milestone S6 — Demonstrate required performance of a representative multichannel sensor after exposure to flight ionizing and non-ionizing radiation environment.

Significance — Demonstrate required sensor performance following full-mission radiation dose. Confirm optimum detector operating temperature. Confirm radiation shielding requirements.

Verification — Laboratory measurement of performance at multiple X-ray energies spanning the required HDXI passband before and after exposure to expected flight levels of ionizing and non-ionizing radiation. (Radiation exposure levels to be determined from recognized environmental models (e.g., SPENVIS).) Demonstrate required operation of sensor (equivalent to one that has achieved Milestone S5 above) at anticipated flight temperature (not across temperature range). Updated sensor performance model predictive capability to include the effects of radiation exposure.

Milestone A1 — Demonstrate single-channel ASIC noise performance at required single-channel rate.

Significance — Establish that required ASIC noise performance can be achieved, and establish preliminary ASIC power requirements.

Verification — Laboratory measurement of an individual ASIC channel with simulated analog sensor input. Develop estimated allocations of total system noise requirements to sensor, ASIC, and other system elements. Demonstrate required single-channel pixel rates based on maximum number of projected channels (sensor technology-dependent). Operational demonstration across the worst-case range of temperatures anticipated in flight (with margin). Confirm power consumption matches analytical ASIC model design projections.

Milestone A2 — Demonstrate ASIC noise performance in multichannel ASIC of representative scale.

Significance — Establish that required ASIC noise performance can be achieved with multiple ASIC channels operating in parallel, and refine ASIC power allocation.

Verification — Laboratory measurement of multiple ASIC channels with simulated analog sensor inputs. Requires (at least provisional) allocation of total system noise requirement to sensor, ASIC, and other system elements. Demonstrate required single-channel pixel rates based on maximum number of projected channels (sensor/ASIC technology-dependent). Operational demonstration across the worst-case range of temperatures anticipated in flight (with margin). Confirm power consumption (laboratory measurement) matches ASIC design model projections (sensor/ASIC technology-dependent).

Milestone A3 — Demonstrate required radiation tolerance.

Significance — Establish the required ASIC noise performance in flight radiation environment.

Verification — Laboratory measurement of multichannel ASIC performance with simulated analog sensor inputs before and after (total ionizing dose and high-LET) radiation exposure using ASIC requirements and measurement conditions used in Milestone A2. (Radiation exposure levels generated using recognized environmental models (e.g., SPENVIS) and expected shielding design). Power consumption and other metrics measured and shown to be consistent with ASIC design model projections (sensor/ASIC technology-dependent).

Milestone Pre-TRL4-5 — Downselection to single technology and TRL 4 certification following SME review.

Significance — At this milestone, a formal downselection from 2 to 1 sensor/ASIC technologies is complete and the selection for development in Phase A is certified to have met the exit criteria for TRL 4.

Verification — Formal decision-making process (e.g., Kepner-Tregoe or Analytic Hierarchy) application with participation of non-advocate SMEs followed by non-advocate TRL 4 certification.

2.3 Milestones for TRL 5

Milestone SA1 — Delivery of brassboard sensor/ASIC unit with multiple pairs from vendor for evaluation following SME review.

Significance — Brassboard electronically verified unit(s) delivered from vendor now available for TRL 5 test sequence.

Verification — Acceptance testing to assure unit is operational—ready for TRL 5 testing.

Milestones SA2 through SA4 — Demonstrate required performance for integrated sensor/ASIC system of representative size.

Significance — Establish that brassboard multiple sensor system performance is achieved with multiple output channels operating in parallel—at least two sensor/ASIC pairs operating in proximity representative of flight configuration.

Verification — Sensor/ASIC unit tested to all TRL 4 exit criteria levels. Extended laboratory testing at multiple X-ray energies spanning the required HDXI passband. Demonstration of acceptable noise and crosstalk levels.

Milestone SA5 — SME review to certify that TRL 4 exit criteria met.

Significance — At this milestone, a formal downselection from 2 to 1 sensor/ASIC technologies is complete, and the selection for development in Phase A is certified to have met the exit criteria for TRL 4.

Verification — Formal decision-making process (e.g., Kepner-Tregoe or Analytic Hierarchy) application with participation of non-advocate SMEs followed by non-advocate TRL 5 certification.

2.4 Milestones for TRL 6

Milestone SA6 — Delivery of engineering model sensor/ASIC unit(s) with multiple pairs from vendor.

Significance — Electronically-verified engineering model unit(s) delivered from vendor, and initial science laboratory testing verifies readiness for engineering model integration and TRL 6 test sequence.

Verification — Acceptance testing to assure unit is operational—ready for TRL 6 testing.

Milestone SA7–SA9 — Demonstrate required performance for 5-sensor focal plane

Significance — Establish that complete system can meet science requirements in relevant environment.

Verification — Full sequence of laboratory testing to demonstrate all performance requirements (sensitivity, noise, power consumption, etc.) at energies spanning the required HDXI passband under space-like conditions (with margin). Correlation with sensor/ASIC model.

Milestone SA10 — Certify Engineering Model at TRL 6 at PDR.

Significance — At this milestone, an engineering model unit will have passed all tests required to meet the TRL 5 exit criteria and the program will be ready to move on to flight-scale sensor/ASIC technology production.

Verification — Formal decision-making process (e.g., Kepner-Tregoe or Analytic Hierarchy) application with participation of non-advocate SMEs followed by non-advocate TRL 6 certification. Acceptance of TRL 6 at PDR

2.5 TRL Development Schedule

The TRL development schedule for HDXI has three major stages: (1) Advancement of HDXI sensors and ASICs from their present TRL 3 to 4, (2) demonstration of integrated sensor/ASIC pairs operating in close proximity and meeting TRL 5 requirements, and (3) demonstration of a fully functional HDXI subarray (5 sensors) of that meets all TRL 6 requirements. The most complex step of TRL development takes place in pre-Phase A (i.e., TRL 3 to 4). As described in §1.3, the

transition from TRL 3 to 4 is estimated to have an AD^2 of 5, and this necessitates the parallel development of multiple (in this case, three) potential sensor technologies at the outset of this phase of the development process. Following the demonstration of TRL 4, technology advancements are expected to involve straightforward (albeit arduous) engineering efforts and the associated AD^2 decreases to the 2 to 3 level.

Although the required performance gains differ for each of the candidate HDXI sensor (and associated ASIC) technologies, they have similar development schedules and budgets, as these are driven by their similar fabrication protocols. Each technology progresses through an iterative cycle of design improvement, lithographic mask production, wafer fabrication and test, device packaging, and laboratory characterization. The duration of this cycle is typically nine months and involves collaboration between semiconductor design and fabrication specialists, fabricators, and university laboratories. Although some overlap of successive cycles is possible (e.g., design work on an improved sensor can begin while characterization of the prior generation continues), only a few cycles can be completed during the pre-Phase A period. Efficient development therefore requires careful planning to fabricate and evaluate appropriate test structures and design variants in each cycle. For these reasons, custom fabrication runs are required for both sensors and associated ASICs to meet the science requirements for *Lynx*. Although the optimized fabrication and development processes are therefore likely to be complex, for concreteness the schedule has been presented as a sequence of consecutive fabrication/test cycles equivalent to the total effort required, which is similar for the three technologies.

Given similar schedules and development protocols, the funding requirements per development cycle for each technology are also similar. Although NASA has invested significantly in these technologies through its Astrophysics Research and Analysis (APRA) and Strategic Astrophysics Technology (SAT) programs, the funding available through these programs alone is insufficient to progress with maximum efficiency. Therefore, although all three sensor technologies are in fact currently being funded (via three APRA grants and one SAT grant), for schedule and budgeting purposes we adopt the conservative assumption that no further progress will be made toward TRL 4 before the start of the pre-Phase A period.

All three technologies will be funded for the first 1.5 years of pre-Phase A development (from 10/1/21 to 4/1/23). This will allow each to complete the equivalent of two fabrication/test runs of both sensors and ASICs. By 4/1/23, there will be a downselect to two technologies. The technologies will be judged on their likelihood to achieve TRL 4. A Kepner-Trego decision process similar to that used successfully to rank *Lynx* Mirror Assembly technologies may be adopted for this purpose. The two highest ranked technologies will then be funded to proceed to TRL 4. These two approved technologies are expected to require an additional fabrication run to achieve TRL 4 by the start of Phase A. Carrying two technologies to this point mitigates risk and allows optimum science return from the HDXI instrument.

One sensor/ASIC technology will be selected for the HDXI before the start of Phase A. For the TRL 5 demonstration, two sensor/ASIC assemblies will be operated in close proximity to simulate co-location in a focal plane. This system will be used to demonstrate required performance after exposure to representative vibration, thermal, and radiation environments. A schedule showing the major milestones (shaded in Table 5) to progress the HDXI technologies to TRL 4–6, as well as major milestone reviews, is shown in Fig. 5.

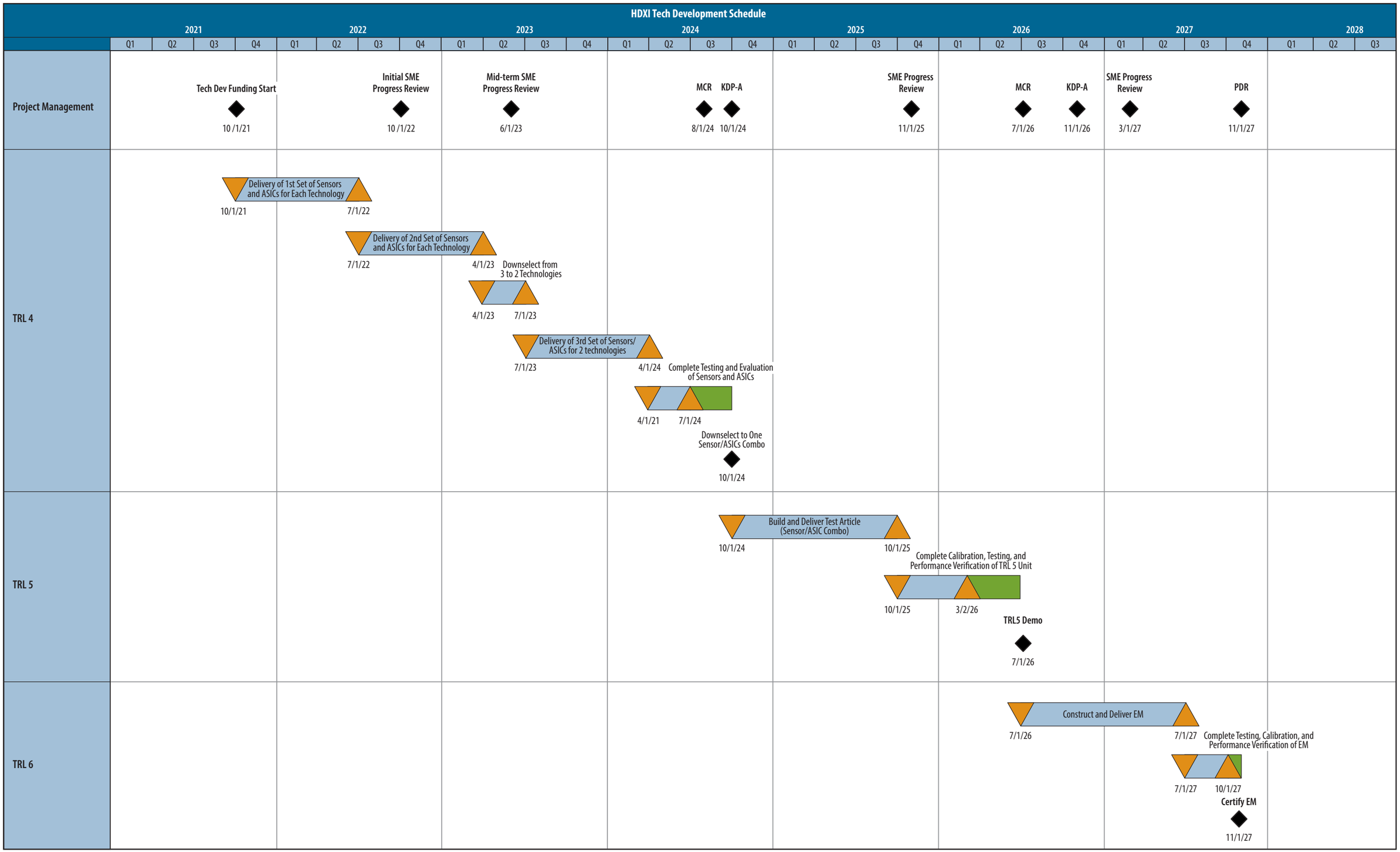


Fig. 5—HDXI technology development schedule to meet TRL 6.

2.6 Cost

Redacted.

2.7 Risks

The *Lynx* study office has performed an in-depth risk assessment with the support of non-advocate SMEs. The assessment has been revisited with each external review and as the various technology development efforts have advanced. The most recent review was performed after the latest PCOS inputs (June 2019). Four significant risks to advancing HDXI to TRL 6 have been identified and are being tracked. Significant risks are defined as those in which either the likelihood or consequence rating was 3 or above. These risks are shown in Table 7. Fig. 6 presents the risk in the standard 5-×-5 format. Brief discussions of each listed risk are provided below.

Table 7—HDXI risk table including mitigation strategies.

Risk #	Risk Title	Risk Statement	Risk Type	Risk Assessment			Mitigation Plan
				L	C	Score	
HDXI-1	Procurement Delays	Vendor delivery schedules for key components (i.e. sensor, ASIC, packaged units) incompatible with Roadmap schedule	S	3	2	6	1. Incentive contracts based on delivery 2. SME-recommended schedule margin 3. Active vendor evaluation by technical and procurement SMEs
HDXI-2	Sensor Performance Requirements Not Met	Noise, framerate, and/or high energy sensitivity specifications required in *Lynx* HDXI requirements table are not met by required date with selected sensor technology	T,S	1	4	4	1. Funded development of 3 sensor technologies with program specified off-ramp criteria/date 2. Multiple scheduled SME reviews for specific intermediate development advances with informal quarterly checkpoints 3. Funded schedule reserve
HDXI-3	Signal Processing Issues	Underestimation of effort to meet signal processing requirements for selected sensor necessitates additional design cycles	T,S	1	3	4	1. Multiple scheduled SME reviews for progress against signal processing metrics with informal monthly oversight 2. Funded schedule reserve
HDXI-4	Unanticipated ASIC Flight Packaging Issues	First flight-type unit does not survive required environmental testing (e.g., vibration and thermal vacuum testing)	S,T	1	3	3	1. Thorough FY21 SME review followed by quarterly SME reviews 2. Development of prototype sensor/ASIC package in TRL 4 to 5 transition period 3. Funded schedule reserve

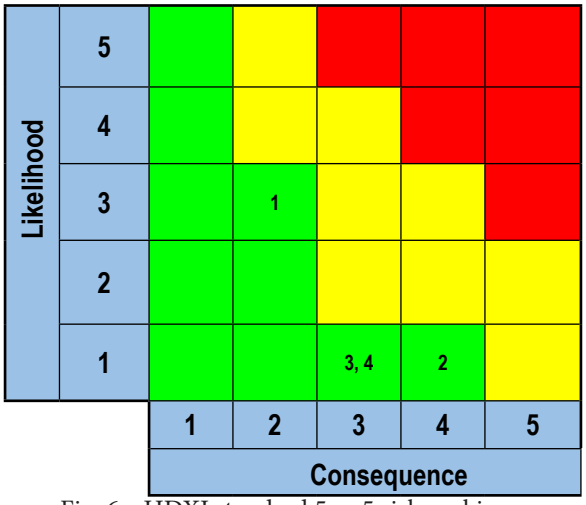


Fig. 6—HDXI standard 5-×-5 risk rankings.

As shown in the table, mitigation strategies have been developed for each risk. One common risk-reduction theme involves interim reviews by SMEs. Past inputs from PCOS and other external

reviewers have indicated concern over a lack of detail leading up to meeting the TRL 4, 5, and 6 exit criteria. In fact, meeting these criteria typically requires multiple iterations with extensive testing at varying levels of fidelity. Interim SME reviews are inserted to assure progress is on schedule or that issues are identified in a timely manner.

Further conservatism is built into the program by the assumption adopted in this roadmap that the pre-Phase A period begins with the SOA at its current level, as described in §1.3. In fact, aggressive development efforts are in progress for each sensor/ASIC system under development, and significant advances may reasonably be expected before the pre-Phase A period begins.

Risk HDXI-1: Procurement Delays — The development of sensors, ASICs, and flight-packaging requires significant fabrication at selected vendors. The vendors have limited production lines and design or vendor schedule changes can result in significant development delays.

Mitigation strategies — In addition to the funded schedule reserve shown in Fig. 5, the program will support active SME reviews of both development activities and vendor capabilities/availability to (1) identify issues/resolutions early in each development cycle to reduce iteration times and (2) identify and recommend optimal scheduling paths. These reviews will occur throughout the development cycle, including the earliest development phases when they could have an impact on technology downselections. The program will also, where possible, implement a contracting strategy that rewards vendors for schedule flexibility and product delivery.

Risk HDXI-2: Sensor Performance Requirements Not Met — As noted in §1 and §1.3, sensor technology development is the key challenge from the combined standpoint of TRL and AD^2.

Mitigation strategies — At this point, three separate sensor/ASIC development paths are funded for risk reduction. While no fundamental barriers to the successful application of any of these three options are known, lessons learned from multiple major programs suggest that assessments of TRL 3 and AD^2 5 make maintenance of multiple technical paths through at least TRL 4 essential to program success (see AD^2 5 definition and GSFC guidelines). The technology roadmap shows planned development of these three options with program-guided downselection criteria (technical and schedule) developed to select a single technology at the beginning of Phase A and development to TRL 6 by PDR. To further reduce risk, there will be quarterly SME oversight (informal) and formal SME reviews (see Fig. 5) to assure that issues are identified and addressed in a timely manner. Further, the schedule includes funded reserve.

Risk HDXI-3: Signal Processing Issues — As noted above, HDXI signal processing requirements are specific to the adopted sensor technology. Because the development efforts are considered straightforward engineering, the schedule shown in Fig. 5 is aggressive, and the need for additional design iterations (e.g., to meet noise and framerate specifications) would result in schedule slip between TRLs.

Mitigation strategies — Quarterly SME reviews (informal) and formal SME reviews (see Fig. 5) are scheduled to catch issues quickly so that iteration cycles (if needed) are minimized with respect to schedule. This is in keeping with the HDXI risk philosophy that timely knowledgeable technical oversight will catch problems quickly and provide for timely collaborative solutions (e.g., technologist not isolated with problems). Planned funded schedule reserve further mitigates this risk.

Risk HDXI-4: Unanticipated ASIC Flight Packaging Issues — While the required flight packaging is not out of family with respect to many advanced instrument development efforts, there will be HDXI-specific technical development issues. These issues are not related to fundamental physical barriers but may require more than one engineering design iteration that would impact the HDXI schedule.

Mitigation strategies — Once a single sensor technology is selected and has met the exit criteria for TRL 4, the transition to TRL 5 will require an intense development program over the next year. To reduce risk in this period, the program will target the development of a prototype ASIC package for environmental testing. If successful, this would exceed the exit requirements for TRL 5 and reduce risk in the TRL 5 to TRL 6 transition. If problems are encountered, minimal TRL 5 exit criteria would still be met and recovery efforts could start at the beginning of Phase B. As with the other HDXI risks, SME oversight (both formal and informal) is scheduled to assure that issues are quickly caught and addressed collaboratively. Funded schedule reserve is also included.

3 Summary

The *HDXI Technology Roadmap* is heavily front-loaded, with significant effort to develop the sensors and the ASICs optimized for this application. Development of large focal planes has considerable heritage in industry, academia, and government laboratories. The process of developing mission-specific pixelated Si sensors has been successfully executed for highly successful astrophysics missions including *Chandra*, *Suzaku*, and *Hubble Space Telescope*, as well as a much larger number of missions outside astrophysics. Known HDXI technology development risks have been quantified with the support of non-advocate SMEs. All risks have specific mitigation strategies based on lessons learned from successful past programs and recent HDXI-specific development efforts. The planned HDXI development is low-risk, and its successful implementation will realize the enormous scientific potential of *Lynx*, providing a powerful new tool for astrophysics.

4 Appendices

4.1 NASA TRL Definitions

TRL definitions per NASA Procedural Requirement (NPR) 7123.1B, Appendix E, are reproduced in their entirety in Table 8.

Table 8—NASA TRL definitions.

TRL	Definition	Hardware Description	Software Description	Exit Criteria
1	Basic principles observed and reported	Scientific knowledge generated underpinning hardware technology concepts/applications.	Scientific knowledge generated underpinning hardware technology concepts/ applications.	Peer reviewed publication of research underlying the proposed concept/application.
2	Technology concept and/or application formulated	Invention begins, practical applications is identified but is speculative, no experimental proof or detailed analysis is available to support the conjecture.	Practical application is identified but is speculative; no experimental proof or detailed analysis is available to support the conjecture. Basic properties of algorithms, representations, and concepts defined. Basic principles coded. Experiments performed with synthetic data.	Documented description of the application/concept that addresses feasibility and benefit.
3	Analytical and experimental critical function and/or characteristic proof-of-concept	Analytical studies place the technology in an appropriate context and laboratory demonstrations, modeling and simulation validate analytical prediction	Development of limited functionality to validate critical properties and predictions using non-integrated software components.	Documented analytical/ experimental results validating predictions of key parameters.
4	Component and/or breadboard validation in laboratory environment	A low fidelity system/component breadboard is built and operated to demonstrate basic functionality and critical test environments, and associated performance predictions are defined relative to final operating environment.	Key, functionality critical software components are integrated and functionally validated to establish interoperability and begin architecture development. Relevant environments defined and performance in the environment predicted.	Documented test performance demonstrating agreement with analytical predictions. Documented definition of relevant environment
5	Component and/or Breadboard validation in relevant environment.	A medium fidelity system/component brassboard is built and operated to demonstrate overall performance in a simulated operational environment with realistic support elements that demonstrate overall performance in critical areas. Performance predictions are made for subsequent development phases	End-to-end software: Elements implemented and interfaced with existing systems/ simulations conforming to target environment. End-to-end software system tested in relevant environment, meeting predicted performance. Operational environment performance predicted. Prototype implementations developed.	Documented test performance demonstrating agreement with analytical predictions. Documented definition of scaling requirements

TRL	Definition	Hardware Description	Software Description	Exit Criteria
6	System/subsystem model or prototype demonstration in a relevant environment.	A high fidelity system/component prototype that adequately addresses all critical scaling issues is built and operated in a relevant environment to demonstrate operations under critical environmental conditions.	Prototype implementations of the software demonstrated on full-scale, realistic problems. Partially integrated with existing hardware/software systems. Limited documentation available. Engineering feasibility fully demonstrated.	Documented test performance demonstrating agreement with analytical predictions
7	System prototype demonstration in an operational environment.	A high fidelity engineering unit that adequately addresses all critical scaling issues is built and operated in a relevant environment to demonstrate performance in the actual operational environment and platform (ground, airborne, or space).	Prototype software exists having all key functionality available for demonstration and test. Well integrated with operational hardware/software systems demonstrating operational feasibility. Most software bugs removed. Limited documentation available.	Documented test performance demonstrating agreement with analytical predictions
8	Actual system completed and "flight qualified" through test and demonstration	The final product in its final configuration is successfully demonstrated through test and analysis for its intended operational environment and platform (ground, airborne, or space)	All software has been thoroughly debugged and fully integrated with all operational hardware and software systems. All user documentation, training documentation, and maintenance documentation completed. All functionality successfully demonstrated in simulated operational scenarios. Verification and Validation (V&V) completed.	Documented test performance verifying analytical predictions.
9	Actual system flight proven through successful mission operations.	The final product is successfully operated in an actual mission.	All software has been thoroughly debugged and fully integrated with all operational hardware and software systems. All documentation has been completed. Sustaining software support is in place. System has been successfully operated in the operational environment	Documented mission operational results.

4.2 AD^2 Definitions

AD^2 is a description of what is required to move a system, subsystem, or component from one TRL to the next. TRL is a static description of the current state of the technology as a whole. AD^2 is what it takes in terms of cost, schedule, and risk to advance to the next TRL. AD^2 is defined on a scale of 1–9 in a manner similar to TRL. The description of the AD^2 levels is shown in Table 9.

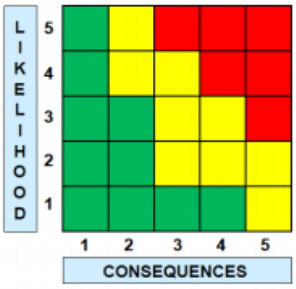
Table 9—AD^2 level definitions.

AD^2	Definition	Risk	Category	Success Chance
1	Exists with no or only minor modifications being required. A single development approach is adequate.	0%		Guaranteed Success
2	Exists but requires major modifications. A single development approach is adequate.	10%		
3	Requires new development well within the experience base. A single development approach is adequate.	20%		
4	Requires new development but similarity to existing experience is sufficient to warrant comparison across the board. A single development approach can be taken with a high degree of confidence for success.	30%	Well Understood (Variation)	Almost Certain Success
5	Requires new development but similarity to existing experience is sufficient to warrant comparison in all critical areas. Dual development approaches should be pursued to provide a high degree of confidence for success.	40%	Known Unknowns	Probably Will Succeed
6	Requires new development but similarity to existing experience is sufficient to warrant comparison on only a subset of critical areas. Dual development approaches should be pursued in order to achieve a moderate degree of confidence for success. Desired performance can be achieved in subsequent block upgrades with high confidence.	50%		
7	Requires new development but similarity to existing experience is sufficient to warrant comparison in only a subset of critical areas. Multiple development routes must be pursued.	70%		
8	Requires new development where similarity to existing experience base can be defined only in the broadest sense. Multiple development routes must be prepared.	80%	Unknown Unknowns	High Likelihood of Failure (High Reward)
9	Requires new development outside of any existing experience base. No viable approaches exist that can be pursued with any degree of confidence. Basic research in key areas needed before feasible approaches can be defined.	100%	Chaos	Almost Certain Failure (Very High Reward)

4.3 Risk Definitions

The standard risk scale for consequence and likelihood are taken from Goddard Procedural Requirements (GPR) 7120.4D, Risk Management Reporting. The definitions for likelihood and consequence categories are provided in Fig. 7.

Likelihood	Safety Estimated likelihood of Safety event occurrence	Technical Estimated likelihood of not meeting performance requirements	Cost Schedule Estimated likelihood of not meeting cost or schedule commitment
5 Very High	($P_{SE} > 10^{-1}$)	($P_T > 50\%$)	($P_{CS} > 75\%$)
4 High	($10^{-2} < P_{SE} \leq 10^{-1}$)	($25\% < P_T \leq 50\%$)	($50\% < P_{CS} \leq 75\%$)
3 Moderate	($10^{-3} < P_{SE} \leq 10^{-2}$)	($15\% < P_T \leq 25\%$)	($25\% < P_{CS} \leq 50\%$)
2 Low	($10^{-5} < P_{SE} \leq 10^{-3}$)	($2\% < P_T \leq 15\%$)	($10\% < P_{CS} \leq 25\%$)
1 Very Low	($10^{-6} < P_{SE} \leq 10^{-5}$)	($0.1\% < P_T \leq 2\%$)	($2\% < P_{CS} \leq 10\%$)



Consequence Categories					
Risk	**1 Very Low**	**2 Low**	**3 Moderate**	**4 High**	**5 Very High**
Safety	Negligible or not impact	Could cause the need for only minor first aid treatment	May cause minor injury or occupational illness or minor property damage	May cause severe injury or occupational illness or major property damage.	May cause death or permanently disabling injury or destruction of property.
Technical	No impact to full mission success criteria	Minor impact to full mission success criteria	Moderate impact to full mission success criteria. Minimum mission success criteria is achievable with margin	Major impact to full mission success criteria. Minimum mission success criteria is achievable	Minimum mission success criteria is not achievable
Schedule	Negligible or no schedule impact	Minor impact to schedule milestones; accommodates within reserves; no impact to critical path	Impact to schedule milestones; accommodates within reserves; moderate impact to critical path	Major impact to schedule milestones; major impact to critical path	Cannot meet schedule and program milestones
Cost	<2% increase over allocated and negligible impact on reserve	Between 2% and 5% increase over allocated and can handle with reserve	Between 5% and 7% increase over allocated and cannot handle with reserve	Between 7% and 10% increase over allocated, and/or exceeds proper reserves	>10% increase over allocated, and/or can't handle with reserves

HIGH RISK

MODERATE RISK

LOW RISK

Fig. 7—Risk matrix standard scale.

4.4 Acronyms

ACIS	Application Specific Integrated Circuits
APRA	Astrophysics Research and Analysis
CAT	Critical Angle Transmission
CCD	Charge-Coupled Device
CMOS	Complementary Metal-Oxide Semiconductor
DDT&E	Design, Development, Test, and Evaluation
DEU	Detector Electronics Unit
DRM	Design Reference Mission
DSMT	Decadal Studies Management Team
EGSE	Electrical Ground Support Equipment
ERP	Event Recognition Processors
FEMB	Front-End Mother Board
FHWM	Full Width at Half Maximum
FOV	Field of View
FPGA	Field Programmable Gate Array
GSFC	Goddard Space Flight Center
HDXI	High Definition X-ray Imager
KDP	Key Decision Point
MCR	Mission Concept Review
MIT	Massachusetts Institute of Technology
OBF	Optical Blocking Filter
PCI	Peripheral Component Interconnect
PCOS	Physics of the Cosmos
PDR	Preliminary Design Review
PPBE	Programming, Planning, Budgeting, and Execution
PSF	Point Spread Function
ROIC	Read-out Integrated Circuit
RMS	Root Mean Square
SAT	Strategic Astrophysics Technology
SIM	Science Instrument Module
SOA	State of the Art
SRR	Systems Requirements Review
STM	Science Traceability Matrix
TRL	Technology Readiness Level
WFIRST	Wide Field Infrared Survey Telescope
XGS	X-ray Grating Spectrometer
XGSRO	X-ray Grating Spectrometer Read-Out

4.5 References

[1] Gaskin, J.A., Swartz, D., Vikhlinin, A. et al., "*Lynx* X-ray Observatory: An Overview", J. Astron. Telesc. Instrum. Syst., 5(2), 021001 (2019). doi:10.1117/1.JATIS.5.2.021001

[2] Falcone, A.D., Kraft, R.P., Bautz, M.W. et al., "Overview of the high-definition x-ray imager instrument on the *Lynx* X-ray surveyor", J. Astron. Telesc. Instrum. Syst., 5(2), 021019 (2019). doi:10.1117/1.JATIS.5.2.021019

[3] Bautz, M., Burke, B., Cooper, M. et al., "Toward fast low-noise charge-coupled devices for *Lynx*",

[4] J. Astron. Telesc. Instrum. Syst., 5(2), 021015 (2019). doi:10.1117/1.JATIS.5.2.021015

[5] Hull, S.V., Falcone, A.D., Bray, E. et al., "Hybrid CMOS detectors for the *Lynx* X-ray Surveyor High Definition X-ray Imager", J. Astron. Telesc. Instrum. Syst., 5(2), 021018 (2019). doi:10.1117/1.JATIS.5.2.021018

[6] Kenter, A., Kraft, R., Gauron, T., "Monolithic CMOS detectors for use as x-ray imaging spectrometers", Proc. SPIE 10762, Hard X-Ray, Gamma-Ray, and Neutron Detector Physics XX, 1076209 (2018). doi:10.1117/12.2322175