MIT KAVLI INSTITUTE

Toward Fast, Low-noise, Low-Power CCDs for Lynx & Other High-Energy Missions

Mark Bautz for

R. Foster, B. LaMarr, A. Malonis, G. Prigozhin, E. Miller, C. Grant ,

MIT Kavli Institute for Astrophysics & Space Research

B. Burke, M. Cooper, D. Craig, C. Leitz, D. Schuette, and V. Suntharalingam

MIT Lincoln Laboratory

Acknowledgements

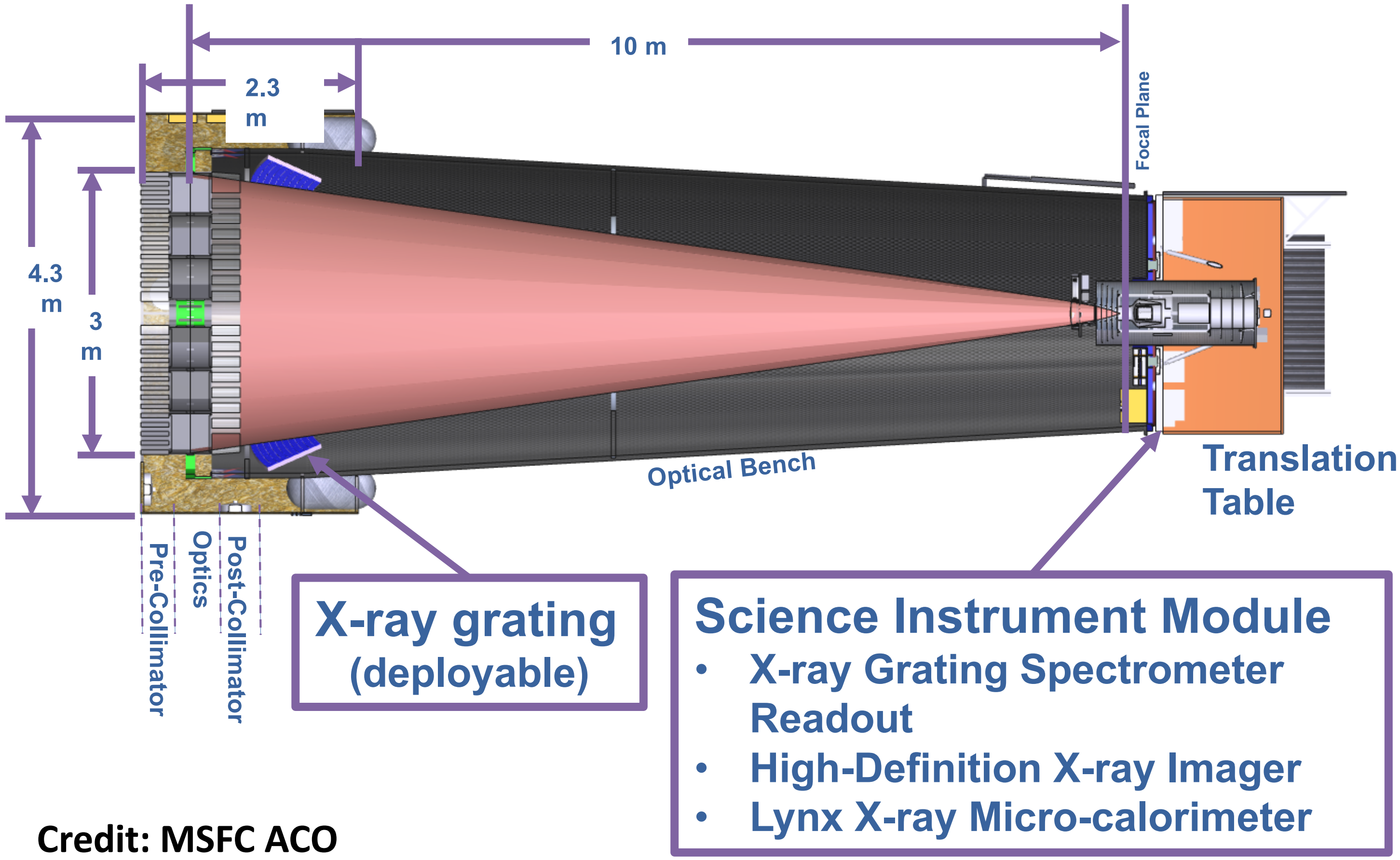
We gratefully acknowledge support for this work from
NASA's Astrophysics Division via APRA and SAT grants to MIT.

The MIT Lincoln Laboratory Digital CCD effort has been supported by the Department of the Air Force.

Overview

- Why consider CCDs for Lynx?
- Advances in CCD technology at MIT Lincoln Laboratory
- Recent measurements of CCD performance
- Challenges for Lynx detectors
  - Small, tall pixels
  - Radiation tolerance
- Next Steps

Lynx Configuration

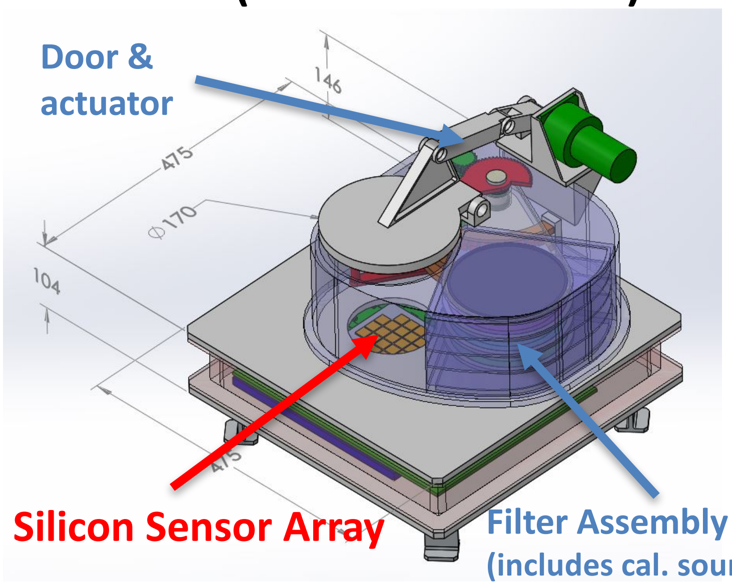


Credit: MSFC ACO

MIT KAVLI INSTITUTE

Silicon Imaging Detectors for Lynx

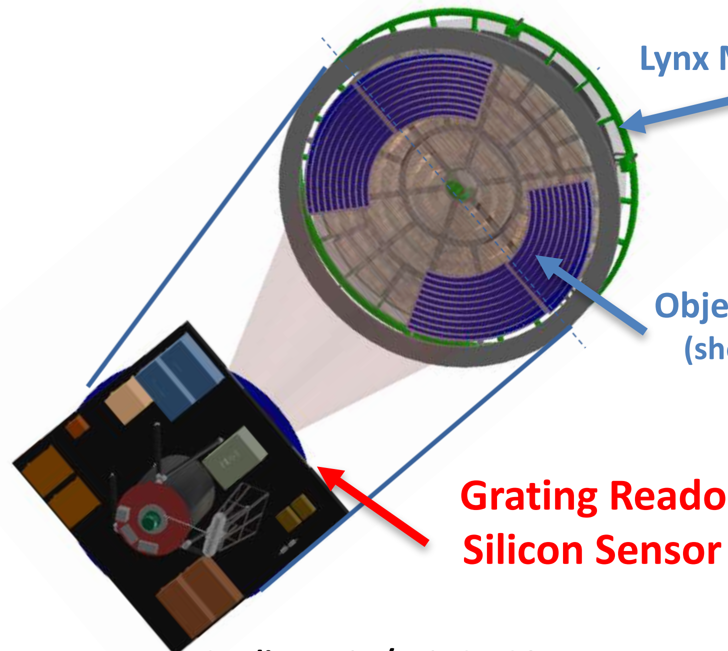
High-Definition X-ray Imager (HDXI)
(Abe Falcone's talk)



Credit: NASA/GSFC IDL

Focus of this talk

X-ray Grating Spectrometer (XGS)
(Moritz Günther's & Randy McEntaffer's talks)



Credit: NASA/MSFC ACO

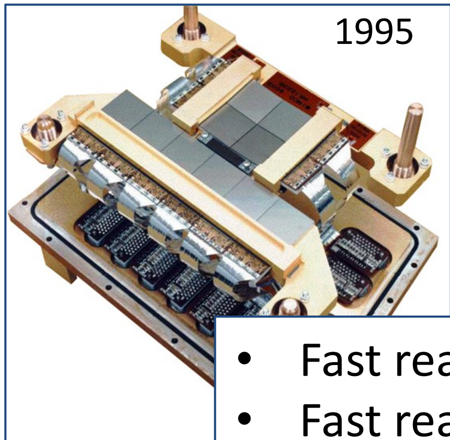
MIT KAVLI INSTITUTE

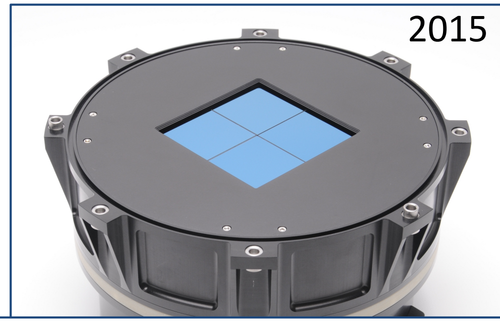
Lynx HDXI Requirements

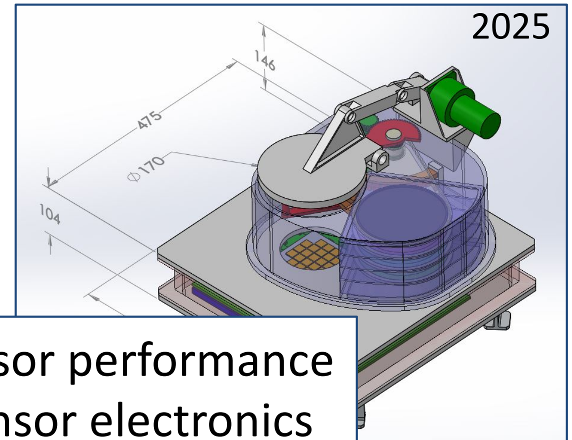
Parameter	Requirement	Remarks
Primary Science Requirements:		
Energy Range	0.3 – 10 keV	***Low energies critical for prime high-z & low kT science***
Field of View	22 x 22 arc-minutes	PSF < 1” HPD over 10’ radius field
Spatial Resolution	Pixels size 0.33 arc-seconds	≤ 16 μm (Lynx focal length = 10m)
Spectral Resolution	60 eV FWHM @ 1 keV	
Derived Requirements:		
Read noise	≤ 4 electrons RMS	**Driven by low-E detection efficiency requirement**
Count rate capability	8000 ct s^{-1}	Full field
Frame Rate	100 frame s^{-1} full field 10^4 windows s^{-1} (~7” x 7” window)	

MIT KAVLI INSTITUTE

What’s so hard about the HDXI focal plane?







- Fast readout + low noise mainly drives sensor performance
- Fast readout + low power mainly drives sensor electronics

Chandra ACIS-I focal plane:

- 2k x 2k, 24 μm pixels
- 45 μm depletion (BI)
- 2-3 e^- read noise
- 0.3 frames s^{-1}
- 40 W; 30 μJ $pixel^{-1}$

TESS focal plane (1 of 4):

- 4k x 4k, 15 μm pixels
- 100 μm depletion (BI)
- < 10* e^- read noise
- 0.6 frames s^{-1}
- < 6W; 0.6 μJ $pixel^{-1}$

Lynx HDXI focal plane:

- 4k x 4k, 16 μm pixels
- 100 μm depletion (BI)
- ≤ 4 e^- read noise
- 100 frames s^{-1}
- ≲50 W; 0.03 μJ $pixel^{-1}$

Why CCDs for Lynx

CCDs:

- Are well-understood
- Have very low noise & excellent uniformity
- Benefit from continuing development

Challenges for conventional CCDs for Lynx:

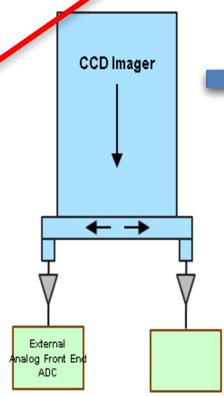
- Readout speed
- CMOS compatibility & power consumption
- Radiation tolerance

Advancing CCD Technology

MIT Lincoln Laboratory “Digital CCD” Program

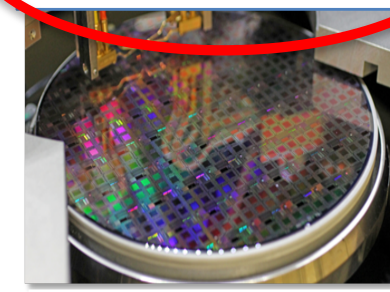
This talk

Chandra-like CCD



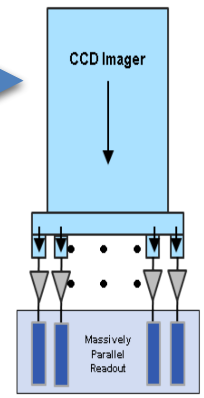
- Simple pixels
- Serial readout
- Low noise at low frame rates
- Large SWaP

Path 1: Develop CMOS-compatible CCD with faster low-noise amplifiers



Path 2: Develop parallel readout & low-power signal chains

Digital CCD



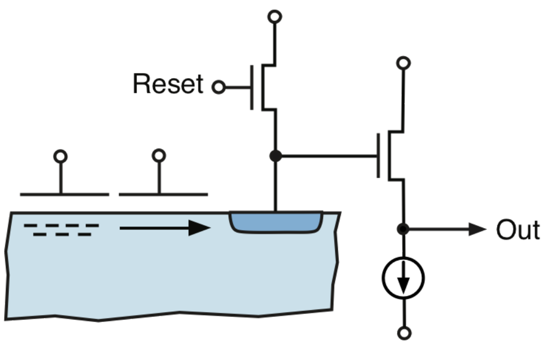
- Simple pixels
- Massively parallel readout
- CMOS compatible clock levels for low SWaP
- Low noise at high frame rates
  - High-speed, low-noise, low-power amplifier
  - Integrated video chain

For Lynx:

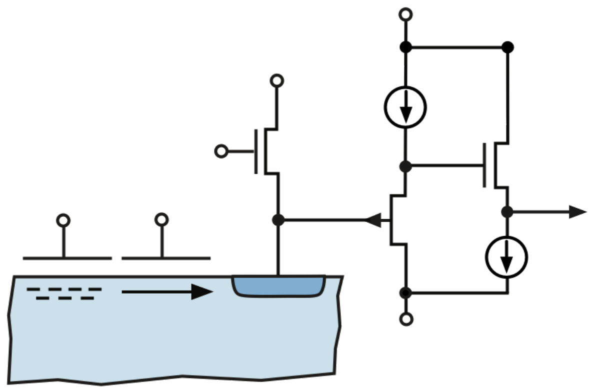
output rate → ~5 MHz

output multiplicity → 32-128/chip

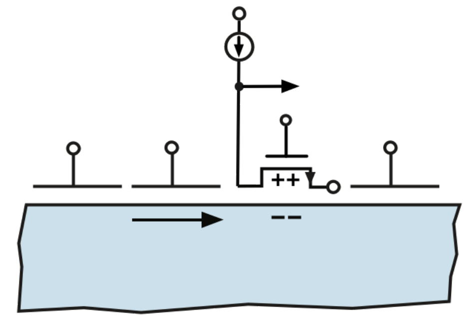
Faster, quieter CCD Amplifiers



nMOSFET



pJFET (with 2nd-stage nMOSFET)



SiSeRO pMOS

Credit: MIT Lincoln Lab.

Chandra/Suzaku

- Low noise
- < 1 MHz

Current (this talk)

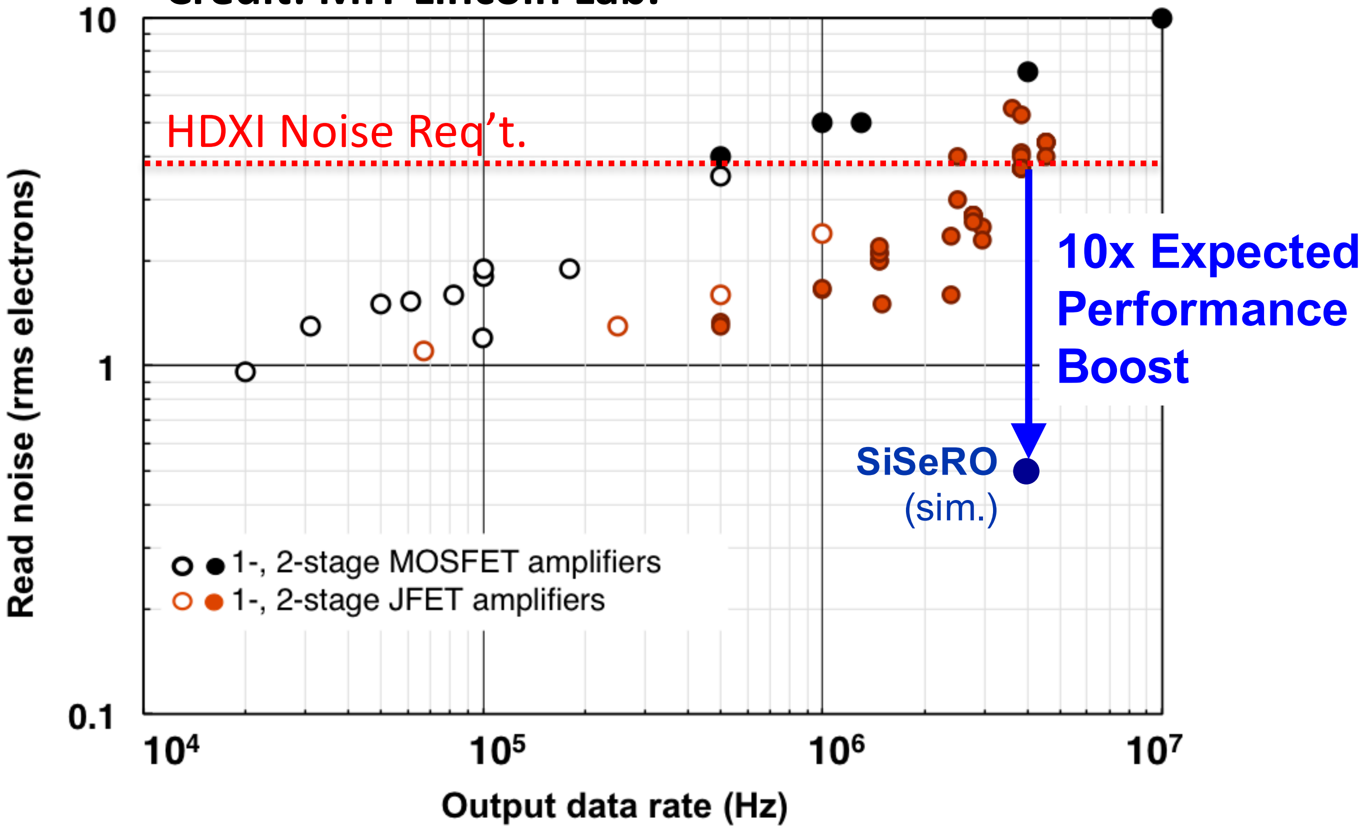
- Low noise
- 1.25 – 5 MHz

In development. Goals:

- Sub-electron noise
- 5 MHz
- Non-destructive read

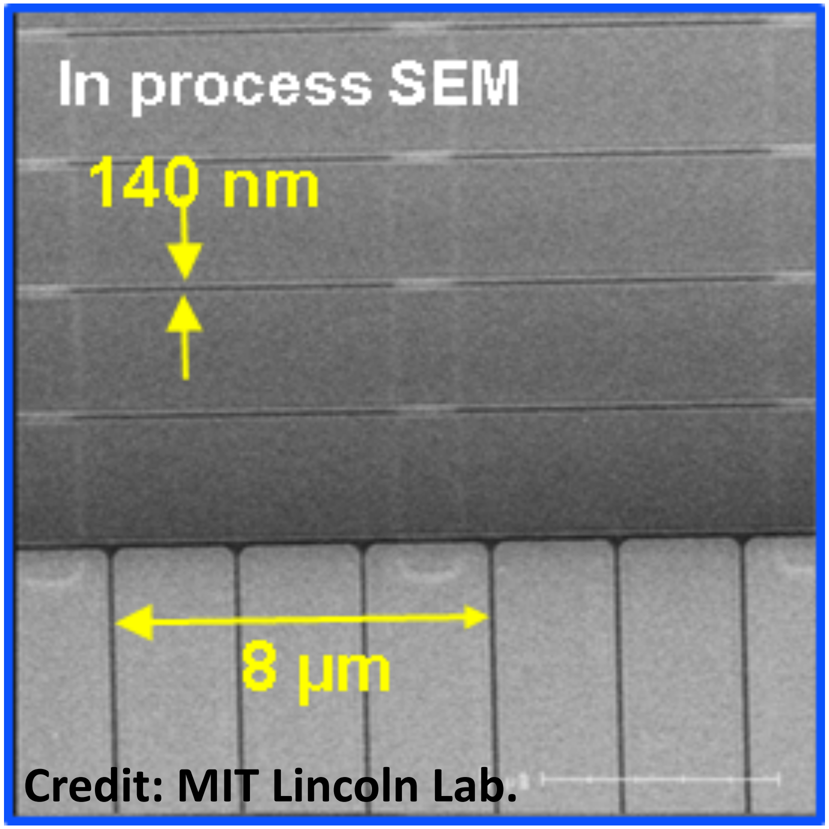
Faster, quieter CCD Amplifiers

Credit: MIT Lincoln Lab.



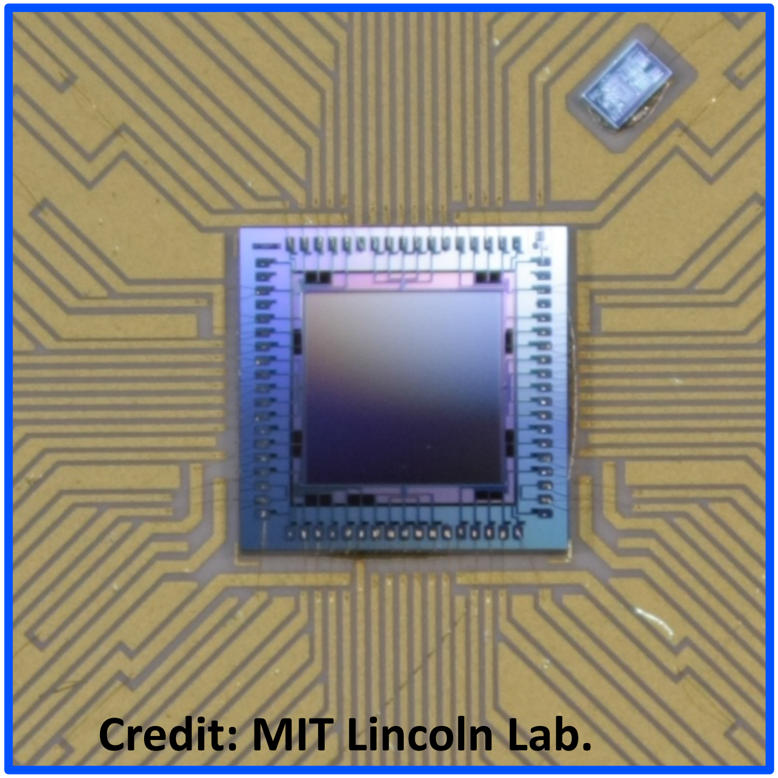
- ○ Chandra/Suzaku
- • Current pJFET
- • In development SiSeRO

CMOS Compatible Charge Transfer



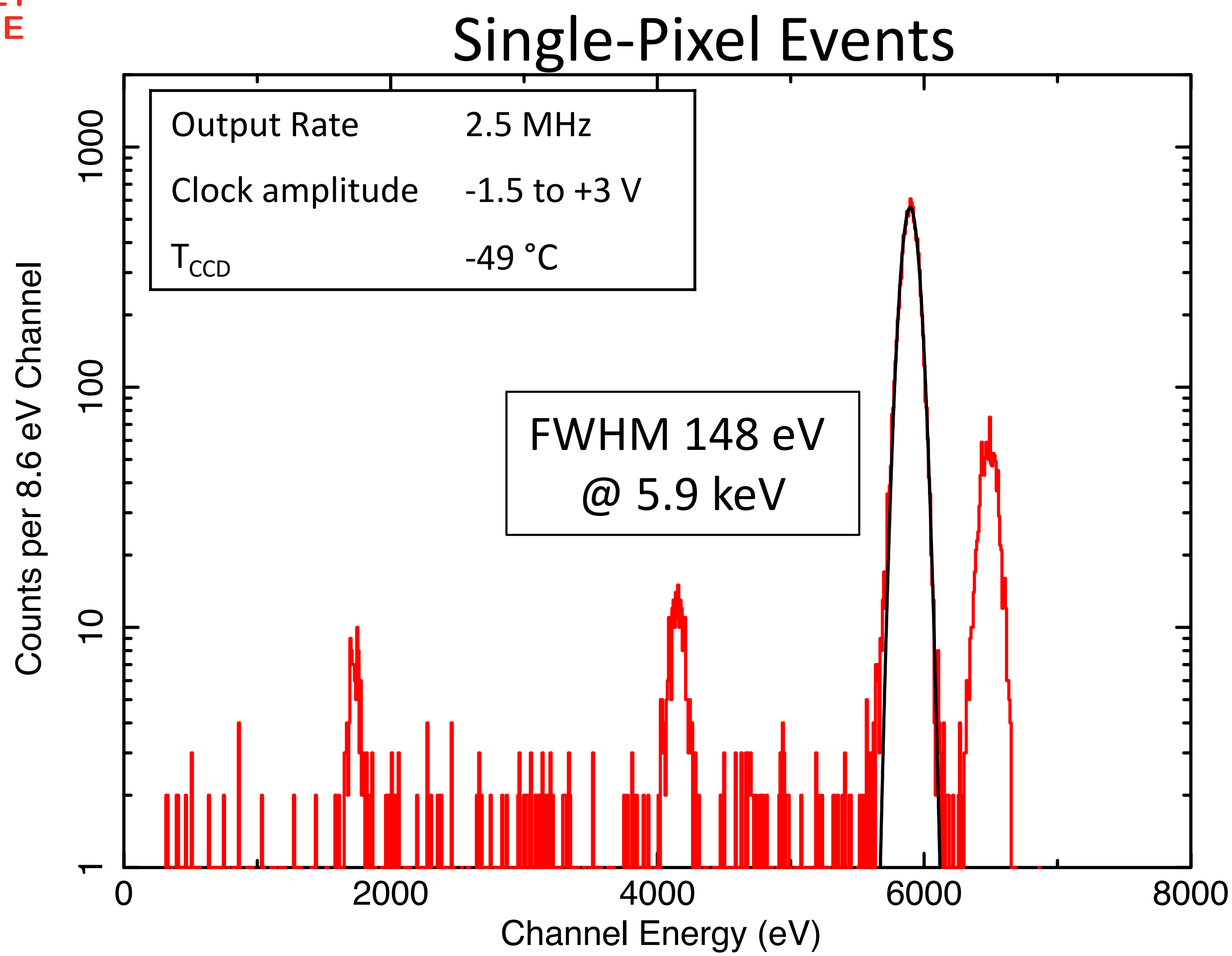
- Single-level polysilicon process + deep submicron lithography
- Provides efficient charge transfer with CMOS compatible clocks swings (± 1.5 V)
- Reduces power required for clocking ($P \sim CV^2f$) by more than 10x

First generation DCCD Test Device (CCID85)



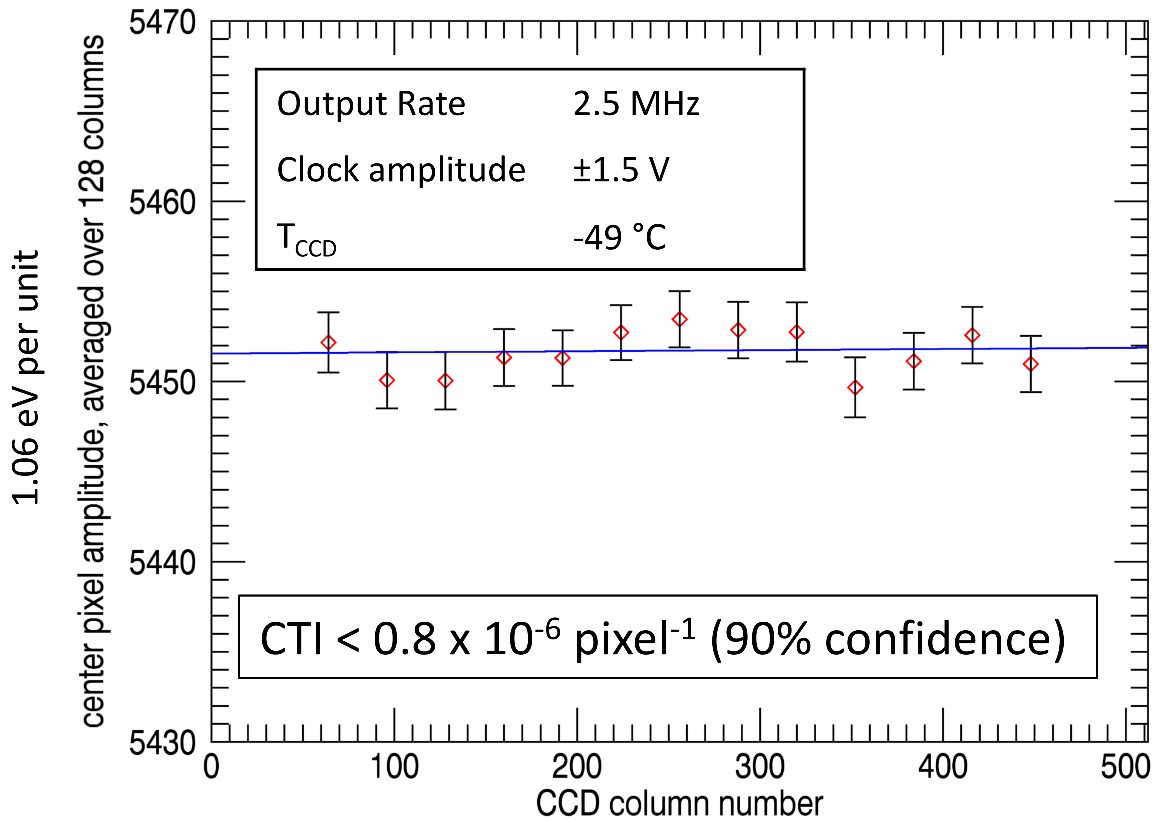
- 512 x 512, 8 µm pixels
- pJFET amplifier (1-5 MHz) & (low-speed) SiSeRO
- Single-poly, CMOS-compatible clocks
- Front-illuminated, ~70 µm depletion

DCCD test results: X-ray Spectrum



DCCD test results: Charge Transfer Inefficiency

Output Register



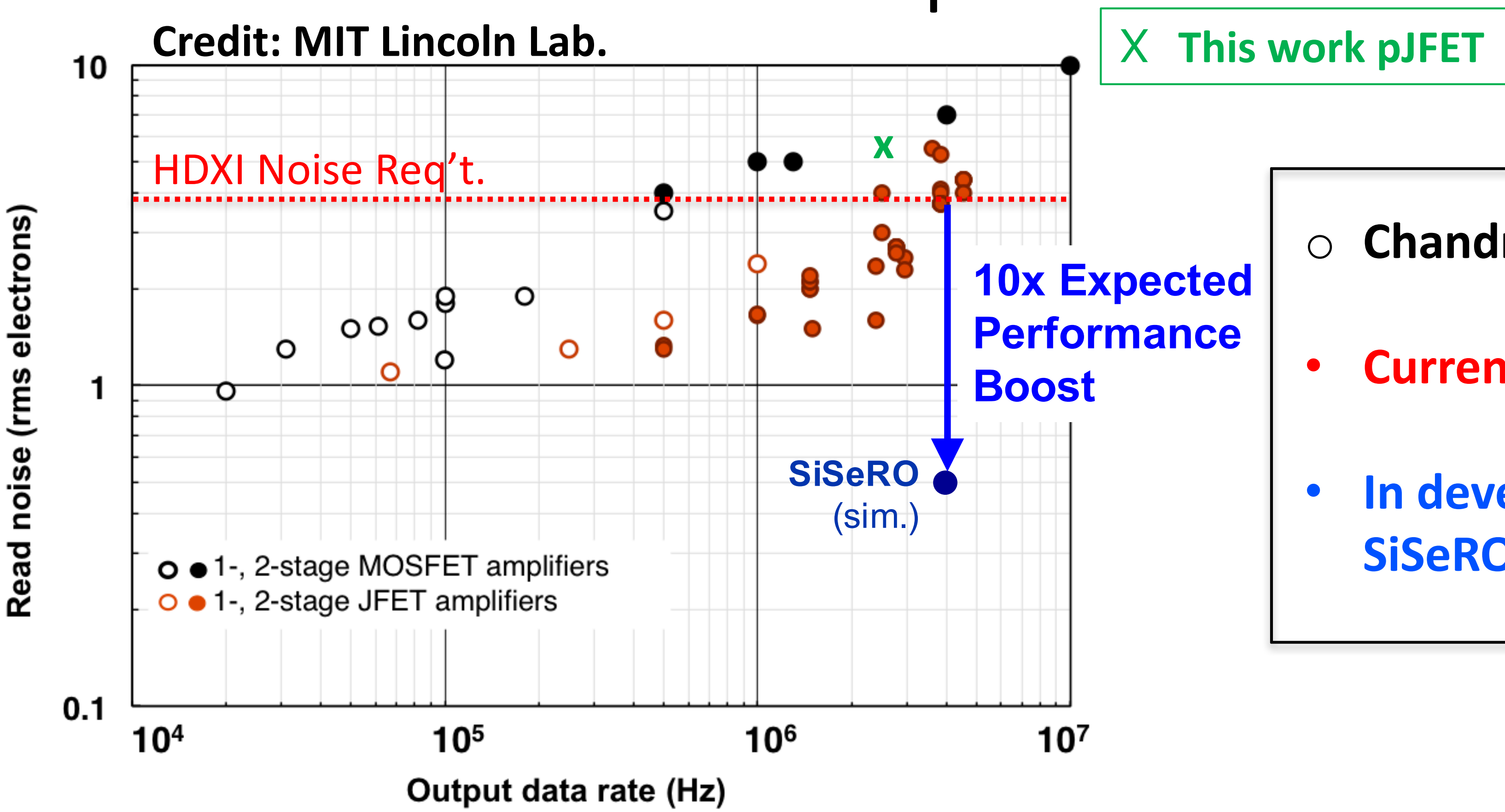
MIT KAVLI INSTITUTE

DCCD Test Results

Parameter	Value	Remarks
Operating conditions:		
Pixel rate	1.25 - 5 MHz	
Clock levels (parallel & serial)	-1.5 V to +3 V (typical) -1.5 V to +1.5 V (CTI measurements)	$\pm$1.5 V is minimum swing allowed by lab electronics
Detector temperature	$-49°$ C	
Measured performance with pJFET amplifier:		
Responsivity	21 μV per electron	
System read noise	6.5 - 7.2 electrons RMS @ 2.5 MHz 10 electrons RMS @ 5 MHz	Includes lab electronics noise of 3.3 electrons RMS
Inferred pJFET read noise	5.5 - 6.4 electrons RMS @ 2.5 MHz 9.4 electrons RMS @ 5 MHz	Excluding lab electronics noise
Spectral Resolution	148 - 151 eV FWHM @ 5.9 keV	single-pixel events
Charge Transfer Inefficiency	Parallel: $(3.0 \pm 1.0) \times 10^{-6}$ per transfer Serial: $< 0.8 \times 10^{-6}$ per transfer	@ 5.9 keV; 90% confidence
Dark current	2.0 electrons per pixel per second	@ -49 °C

Read noise:
5.5 – 6.4 e^-

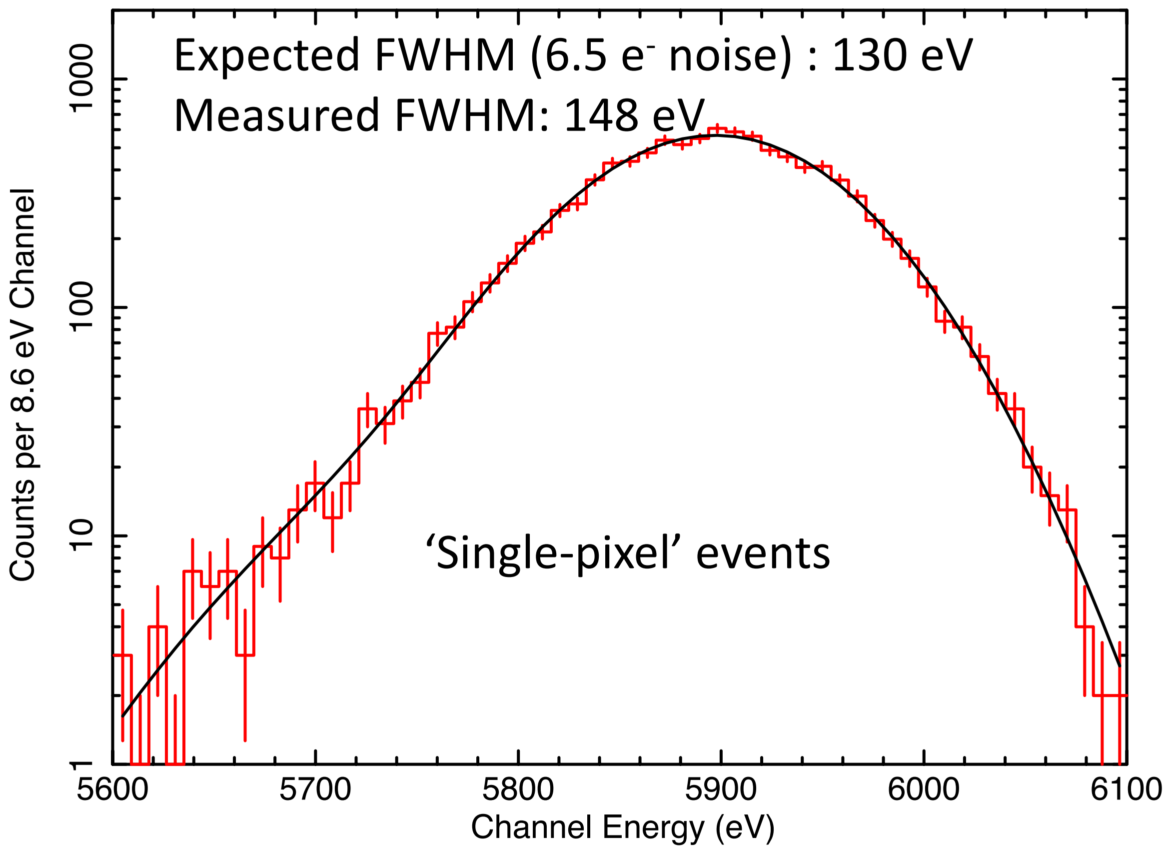
Noise Comparison



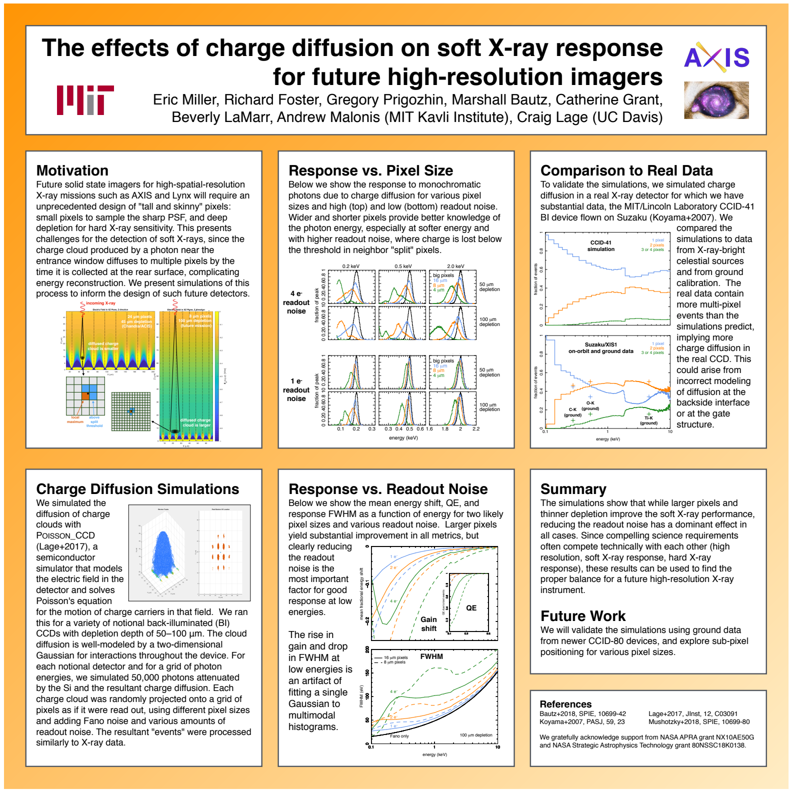
- ○ Chandra/Suzaku
- • Current pJFET
- • In development SiSeRO

Small-But-Tall Pixel Effects

- Similar to HDXI, our test device has relatively small (8 μm) but ‘tall’ (70 μm) pixels
- Charge packets are spread amongst multiple pixels by diffusion
- Consequences for spectroscopy:
    - Multi-pixel events get extra read noise
    - Some charge is lost even from from ’single-pixel’ events
    - Leads to noise-dependent broadening & ’tail’



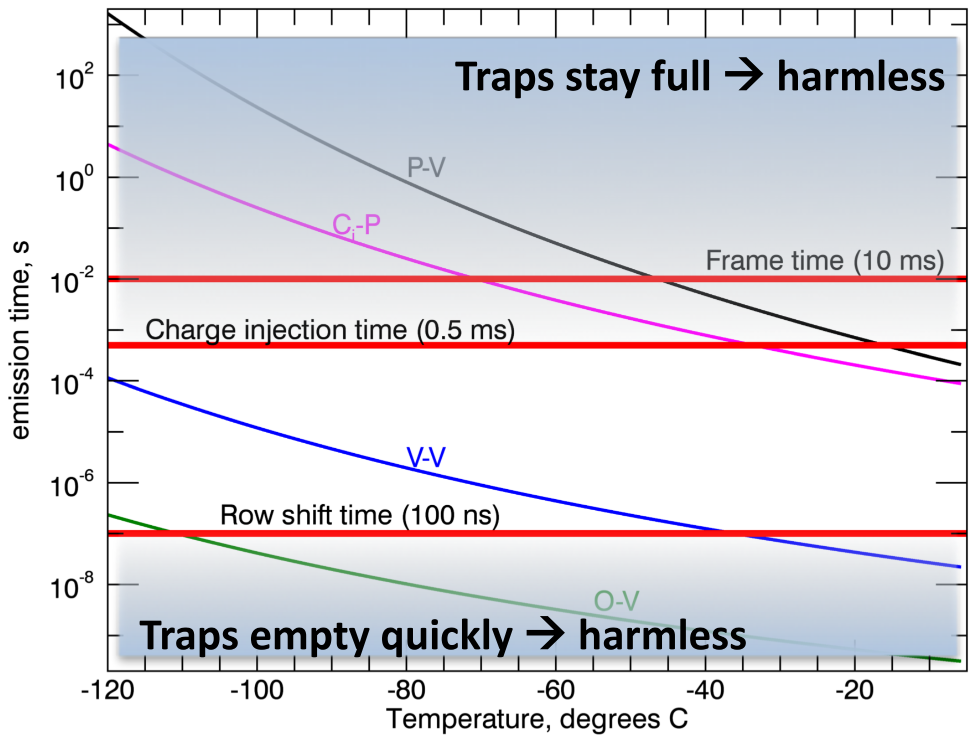
Small-but-Tall Pixel Effects



- Lynx HDXI requires small (16 x 16 μm) but tall (~100 μm) pixels too.
- This will affect both soft X-ray QE as well as spectral resolution.
- May drive noise requirements below present estimates.

See Eric Miller+ Poster 10699-205 THURSDAY!

Radiation Tolerance



G. Prigozhin

- Fast HDXI transfer rates affect CCD radiation tolerance. Only traps with:
  - $0.1\ \mu s < t_{trap} < 0.5$ ms matter for HDXI
- Demonstrated hardening techniques (charge injection, buried channel trough) → satisfactory radiation tolerance for Lynx
- For worst case detector format:
  - **Gain spread of order 10^{-3} yr^{-1}**
  - **FWHM change of order 10^{-2} yr^{-1}**
- We will test these projections!

Next Steps

- Characterize low-speed, high-responsivity SiSeRO amplifier
- Complete fabrication of 2nd generation DCCD test device (shown)
- Features:
  - Back-illumination
  - Frame-transfer architecture
  - pJFET and fast SiSeRO amplifiers
  - Radiation hardening (‘trough’ and charge injection)
- Characterize low-energy response and radiation tolerance

Summary

- MIT Lincoln DCCDs   at 2.5 MHz, with CMOS-compatible clocks, show:
  - FWHM $\lesssim$150 eV at 5.9 keV
  - Noise $\lesssim$ 6 electrons RMS, respsonsivity 21 μV/electron
  - Serial CTI < 0.8×10^{-6}
- Our NASA-funded SAT program is producing next-gen DCCDs to:
  - Demonstrate noise performance required by HDXI (< 4 e^- RMS)
  - Demonstrate soft X-ray (E ~0.3 keV) performance required by HDXI
  - Evaluate radiation tolerance and optimize operating temperature
- DCCDs are an attractive detector technology for Lynx